THE pcb design MAGAZINE

February 2014

AN I-CONNECT007 PUBLICATION

HIGH-SPEED DESIGN

PCB and Packaging Design up to 50GHz:

Identifying Dielectric and Conductor Roughness Models

by Yuriy Shlepnev, Page 12

Alpha Circuit Corp. (formerly Saturn Flex)

Elmhurst, Illinois, U.S.A.

Website | Contact Me | RFQ

ALPHA FLEX SYSTEMS
A DIVISION OF ALPHA CIRCUIT CORPORATION

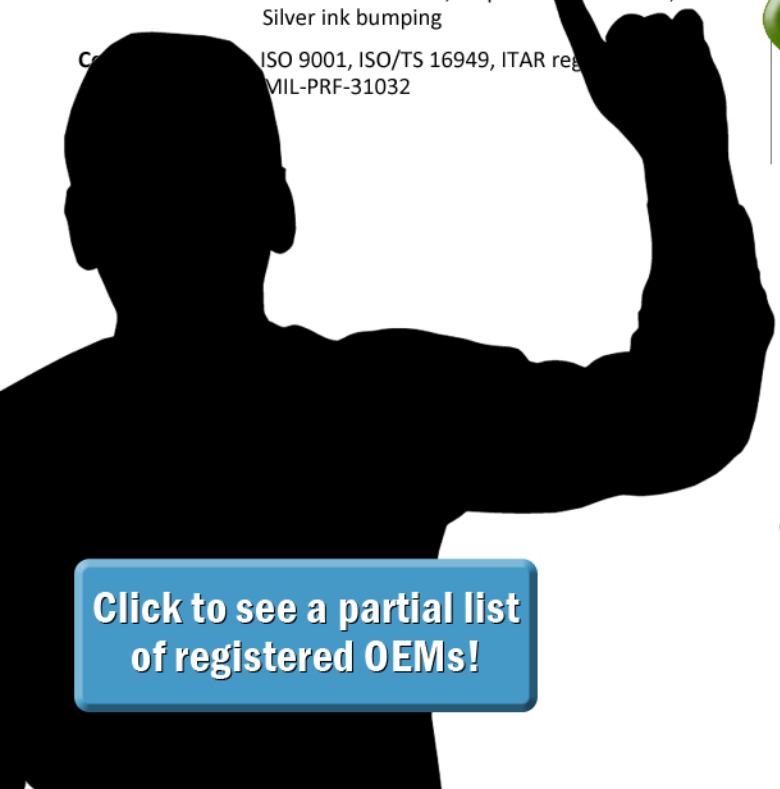
Overview | Contact | Specs | About | Videos | Photos | Brochures | News

The ONLY TS16949 certified domestic Rigid, Flex, and Rigid-Flex bare Printed Circuit Board Manufacturer (NAICS: 334412).

Alpha's FPC / Rigid-Flex PCB manufacturing capabilities continue to grow year-by-year at a rapid rate. Compounding this growth are our increasingly advanced capabilities for rigid PCBs - including open cavities, HDI, sequential lamination, and extreme heavy copper. If there is a demand for a given process, we will make the necessary investments to add capability.

Markets:	Industrial, Military/Aerospace
Board Types:	Double-sided, Flex, Rigid-Flex
Mfg Volumes:	Prototype, Small, Medium
Specialities:	3D Features, Blind/buried via, Heavy copper, Printed Electronics, Sequential lamination, Other: Silver ink bumping
C	ISO 9001, ISO/TS 16949, ITAR re MIL-PRF-31032

Click here to see a demo



Click to see a partial list of registered OEMs!

Why YOU should Showcase:

- Capabilities listing for advanced search functionality
- Specialties and certifications listing
- Ability to upload brochures and videos
- Quick and easy “Contact” and “RFQ” buttons
- News, web and contact links

www.thepcblist.com

Designers: when you choose a fabricator, what guarantee do you have that they won't deliver scrap?

We can connect you with manufacturers that we have audited and are **qualified to deliver the product that you need**, on time and on budget.

How we qualify PCB manufacturers

CLICK TO VIEW

NEXTLEVEL
A PCB AUDITING COMPANY

(360) 531-3495
www.nextlevelpcb.com

THE pcb design MAGAZINE™
February 2014

This Issue: HIGH-SPEED DESIGN

FEATURED CONTENT

What's the state-of-the-art in high-speed design? Find out in this issue of *The PCB Design Magazine,* when our expert contributors Yuriy Shlepnev, Barry Olney and Amit Bahl discuss design on the bleeding edge. And don't miss our coverage of DesignCon 2014.

FEATURE COLUMNS

Discover the Best-in-Class Laminate for High Voltage, Tight-pitch PCB Designs

I-Speed® High Speed Digital Materials

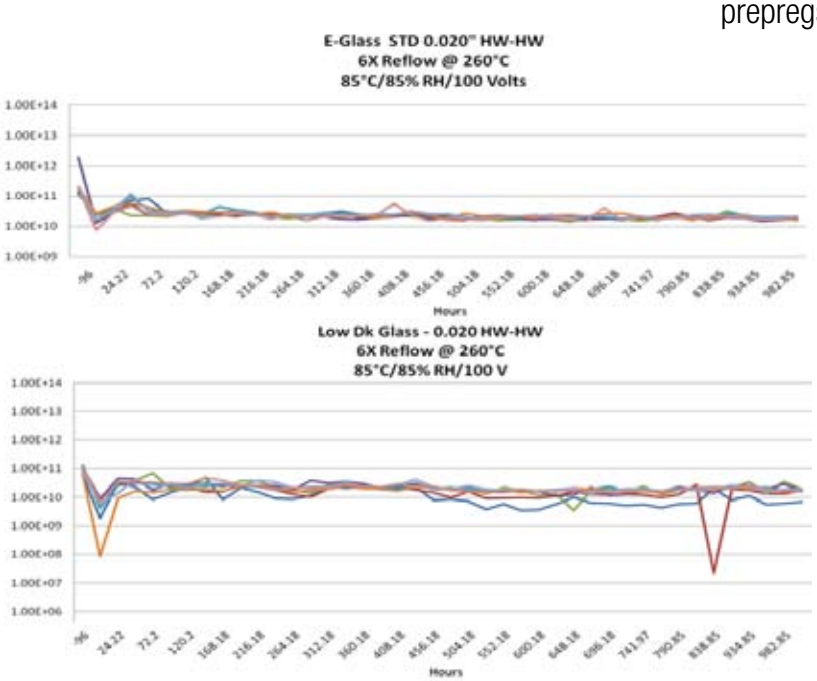
I-Speed laminate and prepreg products are manufactured with Isola's patented high-performance multifunctional resin system, reinforced with electrical grade (E-glass) glass fabric. This system delivers a 15% improvement in Z-axis expansion and offers 25% more electrical bandwidth (lower loss) than competitive products in this space. These properties coupled with superior moisture resistance at reflow, result in a product that bridges the gap from both a thermal and electrical perspective.

I-Speed CAF Test Vehicle Results

- Passed: 85°C/85% RH/100V after 1,000 hours at 0.65 and 0.75 mm pitch
- Passed: 35°C/85% RH/10V after 500 hours at 1.0 mm pitch

I-Speed Features

- Global constructions available in all regions
- Optimized constructions to improve lead-free performance
- Improved Z-axis CTE 2.70%
- IPC 4101 Rev. C /21 /24 /121 /124 /129
- A low Df product with a low cost of ownership
- VLP-2 (2 micron Rz copper) standard offering
- Offer spread and square weave glass styles (1035, 1067, 1078, 1086, 3313) for laminates and prepregs



isola
The Base for Innovation

www.isola-group.com/i-speed

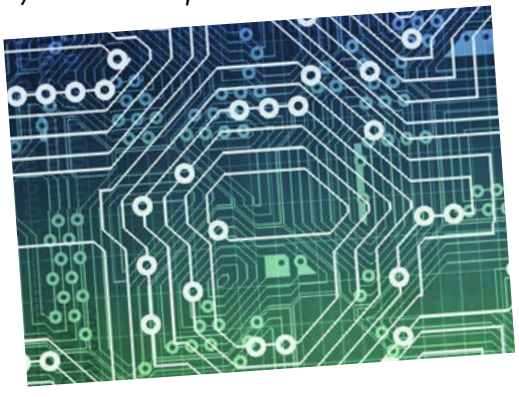
FEBRUARY 2014
VOLUME 3
NUMBER 2
thepcbdesignmagazine.com

THE pcb design MAGAZINE™

THE OPTIMUM MAGAZINE DEDICATED TO PCB DESIGN

AN I·CONNECT007 PUBLICATION

CONTENTS



Mission Critical Reliability

OrCAD is Trusted by the Top 10 Aerospace Manufacturers

Why? Because Cadence® OrCAD® PCB Design tools are industry-proven, highly reliable, and seamlessly integrated. OrCAD provides the complete, rules-driven design and analysis environment necessary to meet the rigorous standards of the aviation industry. Pilots trust their lives to aviation electronics; engineers trust OrCAD.

Click here to learn more about OrCAD

cadence®

EMA Design Automation®

DesignCon: A PCB Design Show

by Andy Shaughnessy
I-CONNECT007

Every DesignCon, we get a chance to check out the current state of PCB (and IC) design, as well as the latest from the EDA tool industry. This year's conference boasted a variety of papers on signal integrity, EMC, test and measurement, and high-speed PCB design in general. There was plenty of focus on 10 Gb Ethernet, and a slew of skew coverage too. I also heard a lot about convergence, such as signal and power integrity capabilities in the same tool environment, and signal integrity and EMC.

The true geeks started off by performing a teardown of their badges to examine the RFID chips that lay behind our names. (I was afraid I'd mess up my badge and have to sneak onto the show floor through a back door. Not that I've ever done that, of course.) It's hard to believe that RFID is cheap enough to be printed onto disposable trade show badges.

Who's working on the next RFID, the next big thing?

Keynote speaker Eileen Bartholomew, senior vice president of prize development for the XPRIZE Foundation, is weighing that same question. The foundation is helping speed the development of new technology by incentivizing innovation with unique, press-grabbing contests. In 2004, the group awarded a $10 million prize to the developers of Spaceship One, which carried three people 100 kilometers into space.

Bartholomew challenged attendees to think in terms of disruptive technology, and to avoid being afraid of failure. And, as she explained, money is a great motivational tool. She pointed out that Charles Lindbergh, a hero of XPRIZE creator Peter Diamandis, was motivated to fly across the Atlantic Ocean by a $25,000 prize offered by hotelier Raymond Orteig.

One $30 million XPRIZE contest challenges private entities—not governments—to land a robot on the moon and send back images and data. Other projects will focus on creating a battery that's up to 1,000 times better than current batteries and tackling illiteracy in children. Lofty goals, all driven by the pursuit of cash. Nothing wrong with that!

The DesignVision Awards were presented, with Altium earning an award for its Altium Designer 14 tool suite. FCI took home an award for its ExaMAX high-speed backplane connector system, as did ANSYS for its PathFinder D technology, its third consecutive DesignVision Award.

On the final day, I moderated a materials panel that covered the development of laminates for speeds up to 50 Gb/s. I was joined by Bryan Nelson of Sanmina, Doug Leys of Park Electrochemical, Dirk Baars of Rogers Corporation, and Fred Hickman of Isola. We discussed the industry's efforts to develop epoxies that are less lossy and suitable for 50 Gb/s and beyond, as well as possible ways to make PTFE more processable for multilayer PCBs. The Q&A period got everyone talking. As one designer said to me before the panel, "PTFE? More like WTF?"

We stayed busy from beginning to end, shooting *Real Time with…* video interviews with

Privately Held Global Printed Circuit Board Fabrication

LOCAL SUPPORT

and a *WORLD* of Circuit Board Manufacturing Options

USA GERMANY JORDAN TAIWAN CHINA

Manufacturing at ANY Volume, both On and Offshore
Quick Turn, Prototypes, DFM, Global Management
Specialties like Rogers, Aluminum, Hybrid Materials
Logistics including Consignment, VMI, JIT & More
24-7 Local Engineering, Service, and Support

Download Digital Brochure

Download Our Capabilities

HT
GLOBAL CIRCUITS

sales@htglobalcircuits.com | (727) 327-6236 | www.htglobalcircuits.com

DESIGNCON: A PCB DESIGN SHOW *continues*

the movers and shakers of PCB design and design engineering. Our guest editors, PCB designer Kelly Dack and DuPont engineer Glenn Oliver, performed above and beyond the call of duty, as usual.

Often, I'd ask Kelly or Glenn out of the blue, "Can you interview this guy for me?" If they were available, they'd do it. Thanks a lot, guys. If you want to see the full *Real Time with...* video program, click here.

Overall, it's hard to ignore the fact that DesignCon is becoming more of a PCB show every year. It wasn't too long ago that this was primarily an IC conference and show. But now, the expo aisles are dotted with booths manned by manufacturers such as Sanmina, Prototron, Sierra Circuits, TTM Technologies, and All Flex, not to mention materials companies like Rogers, Isola, Park and DuPont. And the conference features papers and sessions on signal integrity, EMC, and other PCB mainstays. It definitely helps the PCB design community.

Back to Sin City

Our next big show is IPC APEX EXPO and the Design Forum, which moves back to Mandalay Bay in Las Vegas for 2014 and 2015. We'll be conducting interviews at the Design Forum on Monday, March 24. Design Forum speakers will include IPC's Dieter Bergman, Karen McConnell of Northrup Grumman, Charles Pfeil of Mentor Graphics, Gary Carter of Fujitsu, Ben Jordan of Altium, and Tom Hausherr of PCB Libraries.

Stop by and share your story; we want to hear it. See you in Vegas! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

video interview

Archambault Retired, But Still in EMC

by Real Time with... PCBDesign007

Bruce Archambeault may have retired, more or less. But the IBM emeritus is still working with the IEEE EMC Society, which meets for a symposium this August in Raleigh, NC and in Silicon Valley in 2015.

CLICK TO VIEW

realtimewith.com

Collaborate. Innovate. Accelerate.

Quantum Channel Designer
- Multi-Gigabit Serial Link Design and Analysis

Quantum-SI
- DDR2/DDR3/DDR4 Parallel Bus SI & Timing Analysis

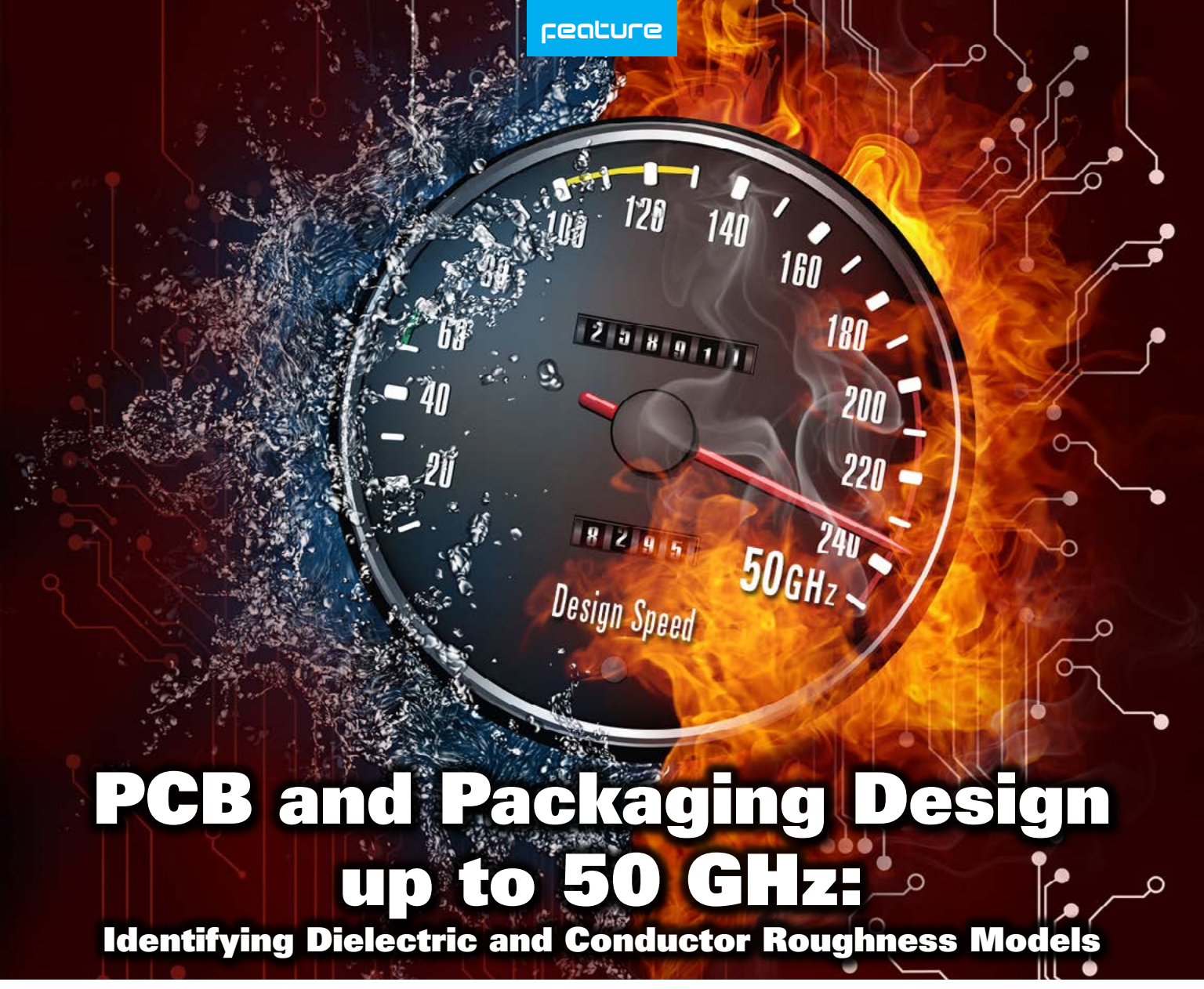
IBIS-AMI Modeling

Consulting Services

SiSoft accelerates design cycles by collaborating with customers and suppliers to develop innovative solutions to the world's toughest high-speed design problems.

SiSoft™
We Are Signal Integrity

www.sisoft.com
978.461.0449



PCB and Packaging Design up to 50 GHz:

Identifying Dielectric and Conductor Roughness Models

by Yuriy Shlepnev
SIMBERIAN INC.

SUMMARY: ***Dielectric and conductor roughness models are necessary for PCB and packaging interconnect analysis up to 50 GHz and beyond. This article provides an overview of a variety of methods for identifying these models.***

Meaningful interconnect design and compliance analysis must start with the identification of broadband dielectric and conductor roughness models. Such models are not available from manufacturers and the model identification is the most important element of successful interconnect design for link paths with 10–50 Gbps and higher data rates. Electromagnetic analysis of interconnects without such models may not be accurate. An overview of broadband dielectric and conductor roughness models for PCB and packaging interconnect problems is provided in the paper. Theory of model identification with generalized modal S-parameters and separation of dielectric and conductor dispersion and loss effects is described. Practical examples of successful dielectric and conductor roughness model identification up to 50 GHz are also provided.

Introduction

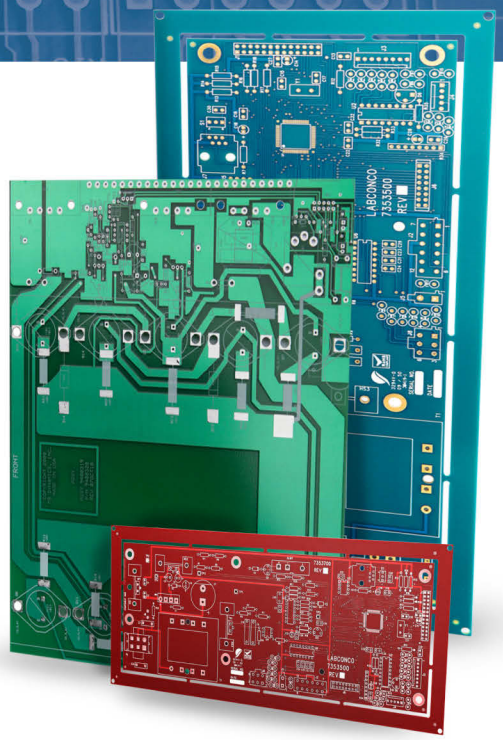
The largest part of interconnects can be formally defined and simulated as transmission line segments. Models for transmission lines are usually constructed with a static or electromagnetic field solvers. Transmission lines with homogeneous dielectrics (striplines) can be ef-

Quality PCBs from the established industry leader

With over 40 years of experience delivering high quality PCB prototypes, Sunstone Circuits® is committed to improving the prototyping process for the design engineer from quote to delivery.

We lead the industry with an on-time delivery rate of over 99%. Plus, our on-site technical support is available every day of the year (24/7/365), giving Sunstone unparalleled customer service.

Get a quote instantly at Sunstone.com



- Live customer support 24/7/365
- Over 99% on-time delivery
- Best overall quality & value in industry
- In business for over 40 years
- Online quote & order
- Free 25-point design review
- RF / exotic materials
- Flex / Rigid-Flex boards
- RoHS compliant finishes
- Free shipping & no NREs
- PCB123® design software
- Controlled impedance testing

SUNSTONE® CIRCUITS

40 YEARS SUNSTONE
40 Years of Serving You

Questions? Sunstone Technical Support is always open: 1-800-228-8198 - support@sunstone.com

fectively analysed with quasi-static field solvers and lines with inhomogeneous dielectric may require analysis with a full-wave solver to account for the high-frequency dispersion[1, 2]. Accuracy of transmission line models is mostly defined by availability of broadband dielectric and conductor roughness models. Wideband Debye (a.k.a. Djordjevic-Sarkar or Swensson-Dermer) and multi-pole Debye models[2] are examples of dielectric models suitable for accurate analysis of PCB and packaging interconnects. Expression for complex permittivity of multi-pole Debye model can be written as follows[2]:

Eq. 1

$$\varepsilon(f) = \varepsilon(\infty) + \sum_{n=1}^{N} \frac{\Delta\varepsilon_n}{1 + i\dfrac{f}{fr_n}}$$

Values of dielectric constant at infinity ε (∞) as well as pole frequencies $f r_n$ and residues $\Delta\varepsilon_n$ are not known for composite dielectrics and have to be identified. The number of poles N for model suitable for analysis of interconnects up to 50 GHz should be 5-10[2].

Expression for complex permittivity of the wideband Debye model can be written as follows[2]:

Eq. 2

$$\varepsilon(f) = \varepsilon(\infty) + \frac{\varepsilon_d}{(m_2 - m_1)\cdot\ln(10)} \cdot \ln\left[\frac{10^{m2} + if}{10^{m1} + if}\right]$$

As in the case of multi-pole Debye model, a number of parameters have to be identified in Eq. 2. Values of m1 and m2 define the position of the first and last pole in the continuous spectrum defined by the model. Those are typically set to very low and very high values outside of the frequency band of interest. Values of ε (∞) and ε_d can be identified with only one measurement of dielectric constant and loss tangent[2]. *f* in Eq. 1 and Eq. 2 is frequency.

To simulate the effect of conductor roughness, Huray's snowball[3] and modified Hammerstadt[4] conductor roughness models can be effectively used. Expression for the conductor surface impedance correction coefficient based on the Huray's snowball model can be written as follows[4]:

Eq. 3

$$K_{rhu} = 1 + \left(\frac{N\cdot 4\pi\cdot r^2}{A_{hex}}\right) \Big/ \left(1 + \frac{\delta}{r} + \frac{\delta^2}{2\cdot r^2}\right)$$

This model has 2 parameters: ball radius *r* and ratio of the number of balls to the base tile area *N/Ahex*. Both are not known for commonly used copper foils.

Another practically useful surface impedance correction coefficient is the modified Hammerstadt model, which can be expressed as follows[4]:

Eq. 4

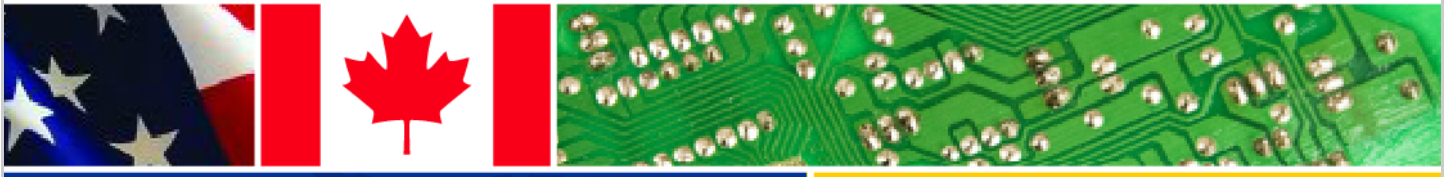
$$K_{rh} = 1 + \left(\frac{2}{\pi}\cdot\arctan\left[1.4\left(\frac{\Delta}{\delta}\right)^2\right]\right)\cdot(RF - 1)$$

It has also two parameters: Δ or surface roughness (SR) parameter (may be associated with RMS peak to valley value) and roughness factor *RF* (maximal possible increase of losses due to roughness). Note that the classical Hammerstadt model has *RF=2* and just one parameter, but this is not very useful for characterisation of PCB copper[4]. δ in Eq. 3 and Eq. 4 is the frequency-dependent skin depth.

Manufacturers of dielectrics usually provide dielectric parameters at 1–3 points in the best cases. It is not possible to construct broadband multi-pole Debye model from just three points, to have model bandwidth from 1 MHz to 50 GHz, as typically required for 10–50 Gbps data links. Five or more points may be required with one of the points close to the highest frequency of interest[2]. In addition, all points have to be consistent and measured with the same method. Manufacturers of advanced PCB dielectric typically provide dielectric constant and loss tangent at 10 GHz or lower frequencies. However, those points may be acceptable for defining the wideband Debye model, because just one point is needed to identify the model parameters. The constructed model be-

In North America

Uyemura is again



#1

for

ENIG
ENEPIG
VIA FILL COPPERS
ELECTROLESS GOLDS

We are honored, and deeply grateful to our customers,
vendor partners and employees for making us North America's leader in PCB finishes. Thank you for an extraordinary year, and for the opportunity to be of service.

As we have since 1985, Uyemura-USA is committed to providing its customers with significant advantages in performance, cost, and maintenance, and to supporting each program with the industry's finest technical support.

UYEMURA
USA

Corporate Headquarters: Ontario, CA · ph:(909) 466-5635 · (800) 969-4842 · fax: (909) 566-5177
Tech Center: Southington, CT · ph:(560) 793-4011 · (800) 243-3564 · fax: (860) 793-4020

comes useful over an extremely broad frequency range.

Things are not so good for the copper roughness models. Manufacturers of copper laminates typically do not offer any parameters for the electrical roughness models. Parameters in datasheets are usable for mechanical purpose, but not for the electrical characterisation. RMS peak-to-valley value Rq can sometime be used for reverse treatment foils as parameter Δ in the modified Hammerstadt model. The roughness factor has to be identified. Thus, meaningful interconnect design and compliance analysis must start with the identification or validation of dielectric and conductor roughness models over the frequency band of interest. Availability of accurate broadband material models is the most important element for design success. Validation or identification of dielectric and conductor models can be done with generalized modal S-parameters[5, 6, 7]. Main steps of the process are described in the next section. Possible methods for separation of dielectric and conductor roughness loss and dispersion effects are also discussed in the paper. Multiple practical examples are provided.

Broadband Model Identification

Dielectric and conductor roughness models identification can be done by matching measured and computed generalized modal S-parameters (GMS-parameters) for a transmission line segment. S-parameters for two line segments with different length and substantially identical cross-sections and transitions to probes or connectors must be measured first to compute measured GMS-parameters. Before proceeding with the identification of the material models, it is important to verify all dimensions of the test structures on the board. In particular, cross-sections of the transmission lines and length difference between two line pairs have to be accurately measured. Next, quality of measured transmission line S-parameters has to be estimated and TDR used to verify consistency of the test fixtures.

The basic procedure for the dielectric and conductors surface roughness models identification is illustrated in Figure 1 can be performed as follows:

(1) Measure scattering parameters (S-parameters) for at least two transmission line segments of different length (L1 and L2) and substantially identical cross-section and conductor roughness profile filled with dielectric with known dielectric model.

(2) Compute generalized modal S-parameters of the transmission line segment difference L=|L2-L1| from the measured S-parameters following procedure described in [5].

(3) Compute GMS-parameters of line segment difference L:

(3a) Guess dielectric (Eq. 1 and 2) or conductor surface roughness (Eq. 3 and 4) model and model parameters.

(3b) Compute generalized modal S-parameter of line segment difference L by solving Maxwell's equations for line cross-section with the broadband material models as described in references 4-6.

(4) Compare GMS-parameters and adjust model to minimize the difference or output the identified model.

(4a) Compare the measured and computed generalized modal S-parameters; compute the metric of difference of two complex GMS-parameters.

(4b) If the difference is larger than a threshold, change model parameters (or model type) and repeat steps 3b-4.

(4c) If the difference is less than or equal to threshold, the dielectric or conductor roughness model is found.

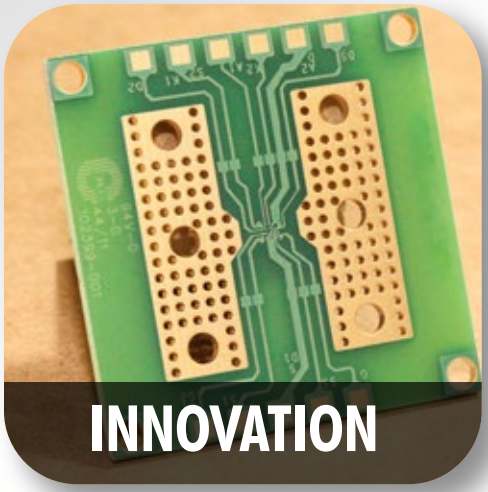
This procedure can be implemented and automated in Simbeor software[8], including the model parameters' optimization. The key in this approach is availability of algorithms for analysis of transmission lines that supports the frequency-continuous material models (Eq. 1-4) in step 3b of the algorithm shown in Figure 1.

It is known that the conductor roughness effect causes signal degradation (losses and dispersion) that are similar to the signal degradation caused by dielectrics[4]. Thus, it is important to properly separate the effects of losses and dispersion between the conductor roughness and dielectric models, or to understand the consequences of not conducting such separation.

CANDOR

Advanced PCB Solutions

WHAT DO WE BRING TO THE RF/MICROWAVE MARKET?
EXPERIENCE. INNOVATION. PERFORMANCE.



Our unique Partial Plating Process enables several copper thicknesses on the same board

Proven track record with RF/Microwave materials like RO6002 and 2929 Bondply

Our unique processes enable us to create solutions that meet the needs of the demanding RF/Microwave market at competitive prices. We use materials from Rogers, Arlon, Teflon, and GETEK depending on the customers requests. We also work with hybrid materials!

WE DON'T JUST SAY IT ...WE CAN PROVE IT!

CLICK TO LEARN MORE

Impedance traces with +-5% or less and highly accurate top-to-bottom registration

Candor Industries, Inc. **www.candorind.com** **416.736.6306**

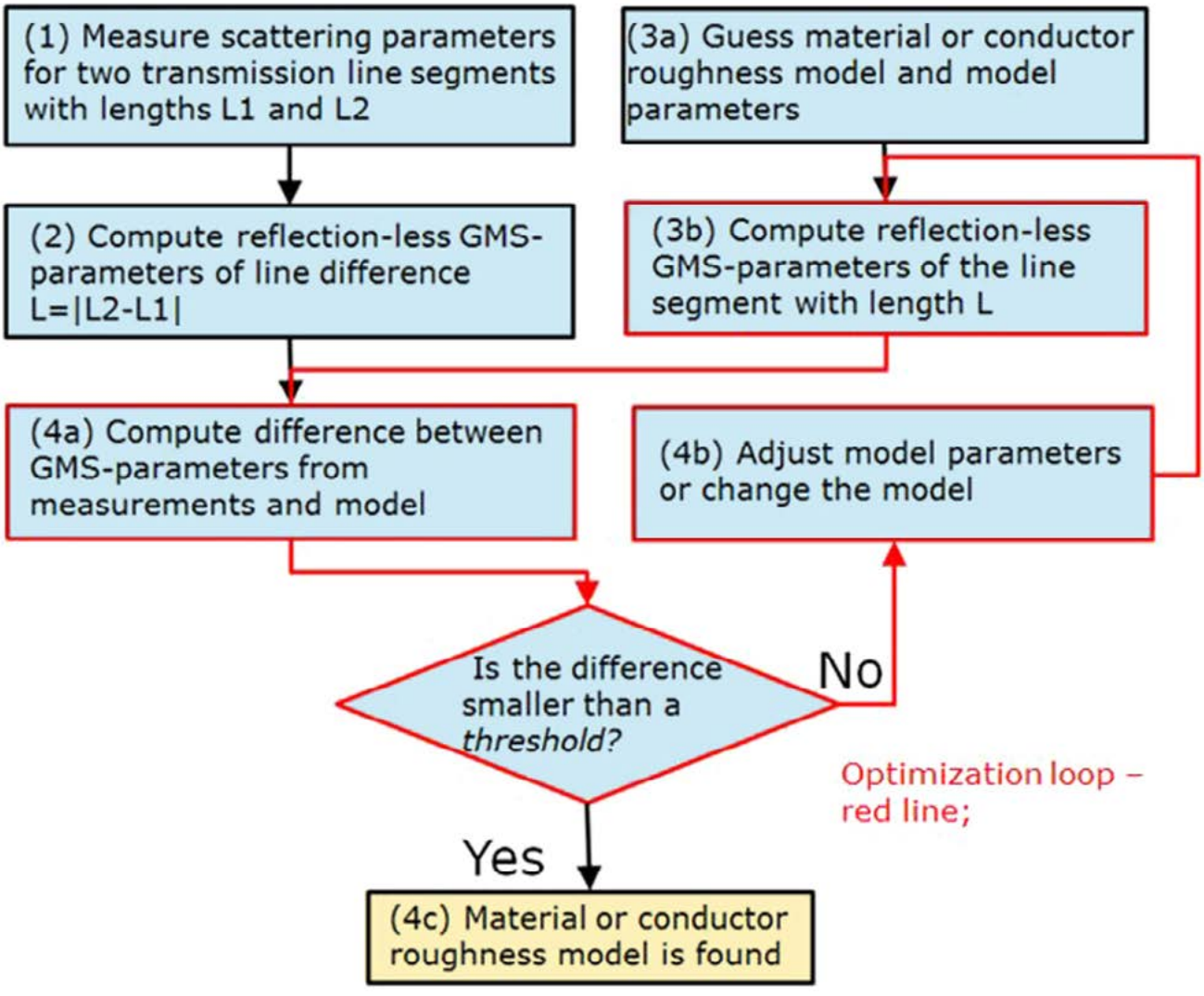


Figure 1: Identification procedure for dielectric material and conductor surface roughness model.

There are four scenarios for building the conductor surface roughness model with and without separation of the loss and dispersion effects between the dielectric and conductor surface roughness models[7]:

1) Optimize dielectric model to fit measured and modeled GMS-parameters following the procedure in Figure 1 and do not use any additional conductor roughness model. The dielectric model will include effect of conductor surface roughness. Such model may be suitable for the analysis of a particular transmission line and has to be rebuilt if strip width or line type is changed. This combined model may be acceptable in cases of high-loss dielectrics when the effect of conductor roughness is minimal. This case is similar to the dielectric model identification described in references 5 and 6, but with rough conductors.

2) Define dielectric model with the data available from the dielectric manufacturer and then identify a roughness model (a roughness correction coefficient) with GMS-parameters following the procedure in Figure 1. This approach works well if a manufacturer has reliable procedure to identify the dielectric properties (most of them do). Wideband Debye models can be defined with just one value of dielectric constant and loss tangent specified at one fre-

INTRODUCING COOLSPAN® TECA

thermally & electrically conductive adhesive

Rogers can help by being your reliable conductive adhesive film source

Get the heat out of those high-power PCBs. COOLSPAN® Thermally & Electrically Conductive Adhesive (TECA) Films are ideal for dissipating heat in high-frequency circuits. COOLSPAN adhesives feature outstanding thermal conductivity (6 W/m/K) and reliable thermal stability. Keep things cool, with Rogers and COOLSPAN TECA film.

CONTACT YOUR SUPPORT TEAM TODAY

Visit Us At APEX EXPO IPC Booth #1828

ROGERS CORPORATION www.rogerscorp.com

MEET YOUR COOLSPAN® TECA FILM SUPPORT TEAM

Leading the way in...

• Support • Service • Knowledge • Reputation

SCAN THE CODE TO GET OUR CONTACT INFO.

Greg Bull
Applications Development Manager *Northern Territory (U.S.) & Canada*

Dale Doyle
Applications Development Manager *Western Territory (U.S.)*

John Dobrick
Applications Development Manager *Southern Territory (U.S.) & South America*

Scott Kennedy
Applications Development Manager *Eastern Territory (U.S.)*

John Hendricks
European Sales Manager

Kent Yeung
Regional Sales Director *Asia*

If you are unable to scan a VR code please visit our Support Team website at www.rogerscorp.com/coolspan

quency point[5]. This is the simplest way to identify the conductor roughness model.

3) If the dielectric model is not available, identify dielectric and conductor roughness models separately. In addition to two line segments with rough copper, make two or more transmission line segments with flat rolled copper on the same board. First, use segments with flat copper to identify parameters in dielectric model following the procedure in Figure 1. Then use the identified dielectric model for rough segments and identify the conductor roughness model following the same procedure Figure 1, but for the roughness model. This is the simplest way to separate loss and dispersion effects in conductor surface roughness and dielectric models.

4) If the dielectric model is not available, identify dielectric and conductor roughness models simultaneously. It can be done with multiple line pairs with different widths of strips in each pair (narrow, regular and wide strips made of the same rough copper for instance). Dielectric model and conductor roughness model parameters can be optimized simultaneously following the procedure in Figure 1, until differences of GMS-parameters for segments of all strip widths reach the stopping criteria. The resulting dielectric and roughness models will be usable for a given range of the strip widths. Though the procedure is the most complicated and may lead to multiple possibilities (ambiguities).

Overall, the material identification procedure described here is the simplest possible. It needs measurements for 2 t-lines with any geometry of cross-section and transitions. No extraction of propagation constants (Gamma) from measured data is required. The extraction of Gamma is difficult and error-prone. Also, no de-embedding of connectors and launches is required. De-embedding of PCB structures is usually difficult or even impossible due to inhomogeneity of dielectrics and manufacturing variations. The approach needs the simplest numerical model—only propagation constant has to be computed for a given cross-section and with the material models to identify. No 3D electromagnetic models of the transitions

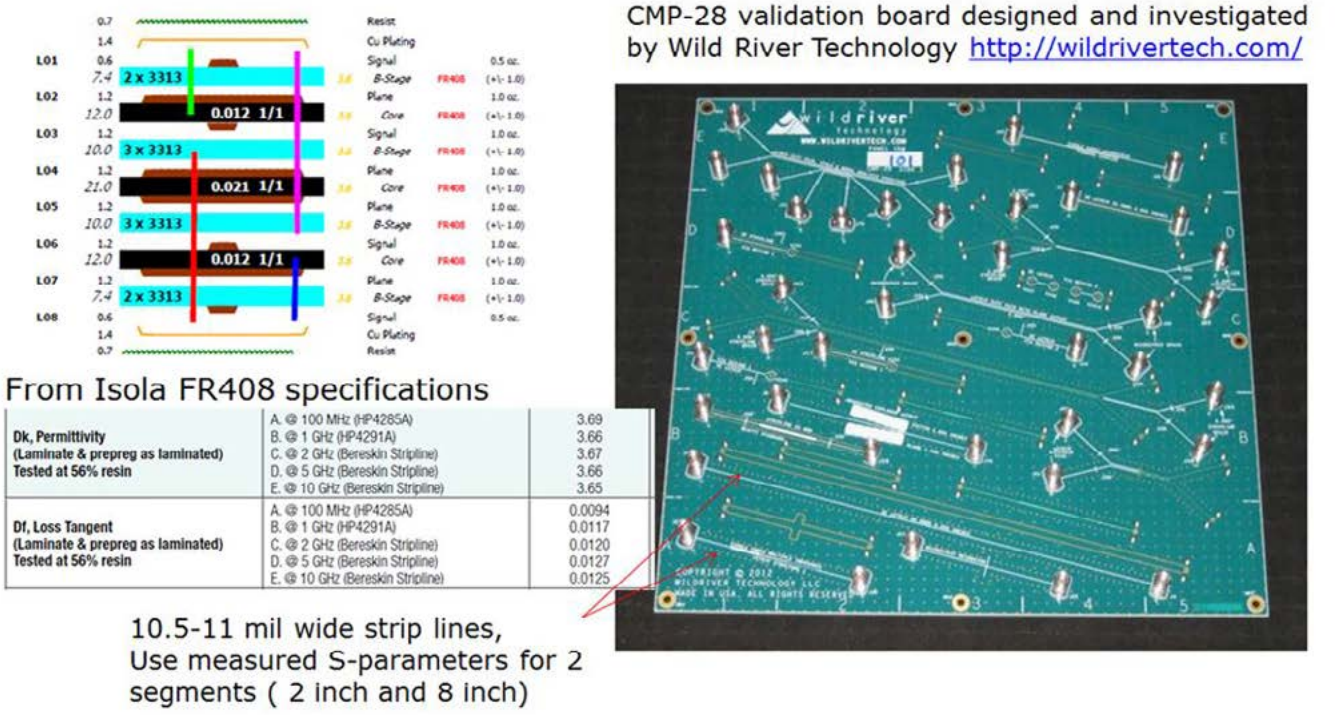


Figure 2: A CMP-28 board stackup and view. Dielectric parameter data from manufacturer also shown.

are required. Procedure with GMS-parameters has minimal number of smooth complex functions to match during the identification process. Specifically, one S-parameter for single and two S-parameters for differential lines have to be matched. All reflection and modal transformation parameters are exactly zeroes. Identified models are frequency-continuous and models (Eq. 2–4) are not restricted to the frequency band used in the identification process—they are naturally extendable above the upper frequencies and below the lower frequencies.

Practical Example

As an example of material parameters identification up to 50 GHz (for 25–50 Gbps data channel) we use measured data provided by Wild River Technology for CMP-28 channel model platform validation board made with Isola FR-408 materials and regular copper.

The board and stackup are shown in Figure 2. Five points for dielectric constant and loss tangent are available from the datasheet for the FR-408 material, but the points are measured with different methods and the maximal frequency is only 10 GHz. Frequency-continuous multi-pole Debye model cannot be accurately defined up to 50 GHz with those data. No data for the conductor roughness was available from the board manufacturer. To identify dielectric and conductor roughness model parameters, we can use 2-inch and 8-inch single-ended stripline links in layer L03 (see stackup in Figure 2).

S-parameters measured for two line segments are shown in Figure. 2.

Following the procedure outlined in the previous section, we first estimated measured S-parameters quality in Simbeor Touchstone Analyser tool[8]. As we can see from Figure 3, the quality of S-parameters for the stripline segments is excellent (final quality metric is close to 100%). TDRs of both segments have been also evaluated and both links looked consistent (impedance and discontinuities are close). After measured S-parameters for test structures were pre-qualified, we convert the measured reflective S-parameters into generalized or reflectionless S-parameters shown in Figure 4 (red and blue curves).

Dielectric specifications (see insert in Figure 2) show that this dielectric has dielectric constant (Dk) 3.66 and loss tangent (LT) of 0.0117 at 1 GHz (the other points are also consistent with that value and WD model). We can use that point to define the wideband Debye model (Eq. 2). If we compute GMS-parameters for 6-inch segments with the electromagnetic analysis with wideband Debye model and Dk=3.66 and LT=0.0117 defined at 1 GHz (shown with blue curves in Figure 4), the difference in the measured and computed group delay is relatively small, but the difference in GMS insertion loss is large, up to 25% as shown in Figure 4.

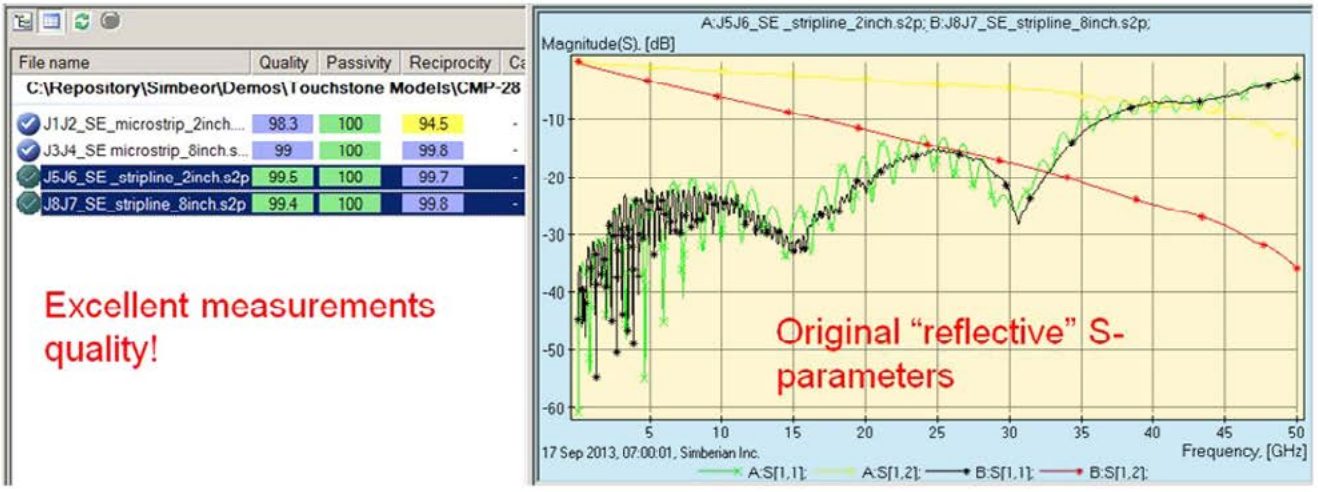


Figure 3: Measured S-parameters for two stripline links and quality evaluation.

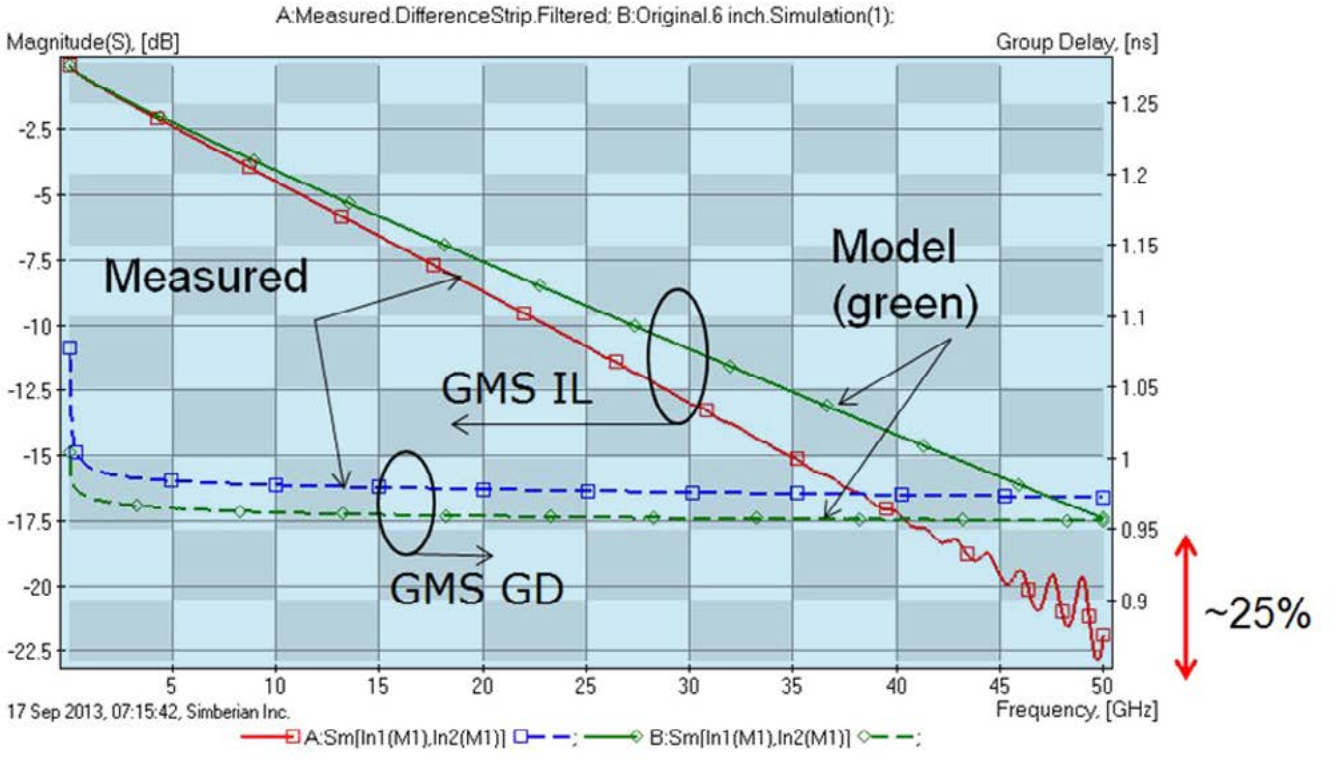


Figure 4: Measured (red and blue curves) and computed (green curves) generalized modal insertion loss (left plot) and group delay (right plot) for 6-inch stripline segments (dielectric model from manufacturer and smooth conductor model).

Dk in the model must be increased to 3.83 to match the measured group delay—that increase can be explained by the layered structure and anisotropy of the dielectric due to that. How to explain the large difference in the predicted and measured insertion loss? Typically this situation is attributed to incorrect data from the manufacturer. In this case, LT should be increased to 0.0138 to have an acceptable match for the insertion loss. With such adjustment, the measured and computed GMS-parameters match well as shown in Figure 5.

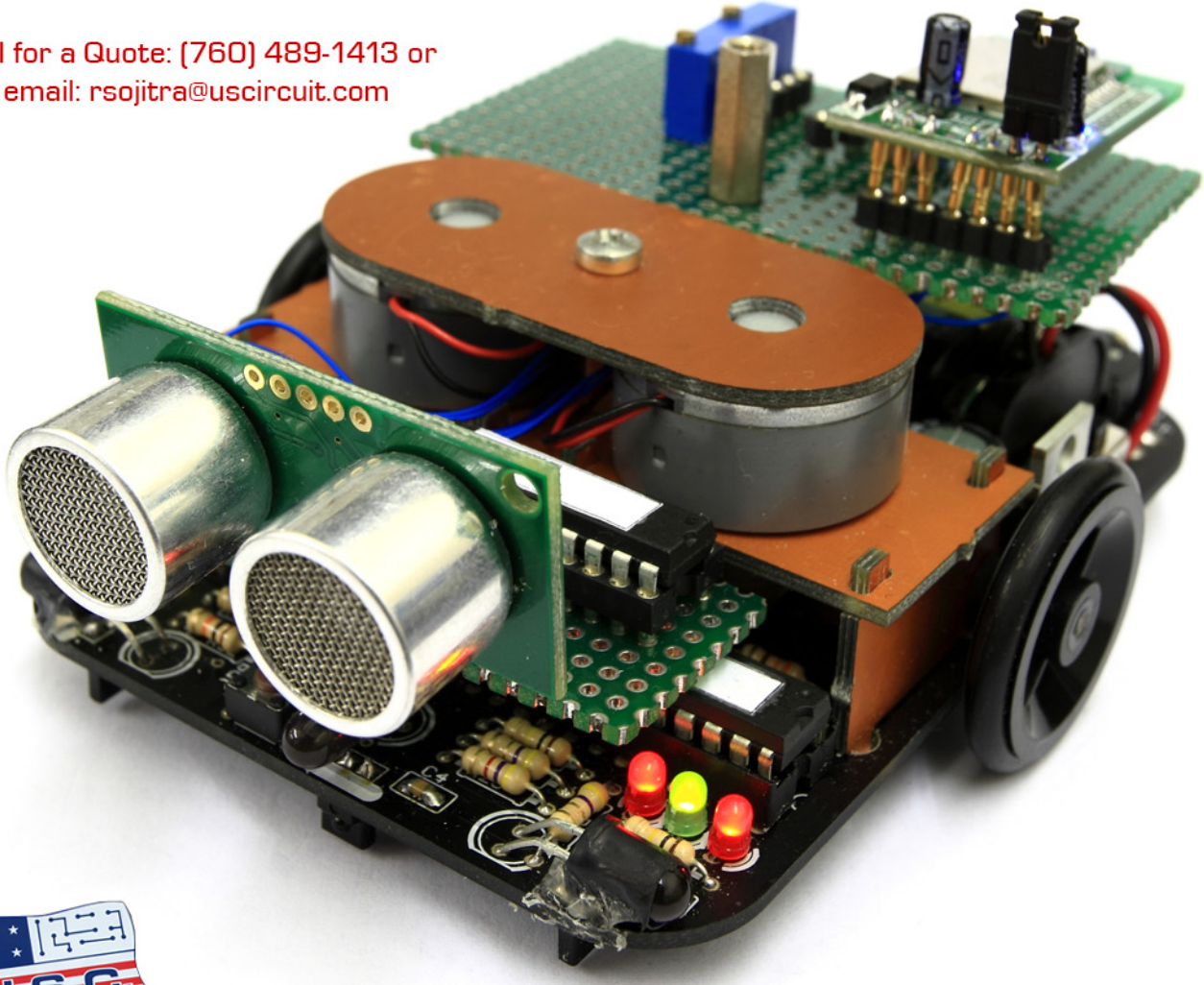
Another option is to assume that the dielectric loss tangent from the manufacturer datasheet is actually accurate enough (it is typically measured with the accurate strip resonator method and strips are made of smooth copper), and attribute all observed excessive losses to the conductor roughness. As shown in Figure 6, nearly perfect correspondence of measured and computed models can be achieved with the modified Hammerstadt model (Eq. 4) with the roughness parameter 0.32, roughness factor 3.3 and conductor resistivity adjusted to 1.1 (relative to resistivity of annealed copper). To match the GMS group delay, smaller adjustment of the dielectric constant from 3.66 to 3.8 was needed.

As the result of this simple example we ended up with two models—one with the conductor roughness effect accounted by increase of dielectric loss tangent from 0.0117 to 0.0138, and another model with loss tangent 0.0117 as in the specs and additional modified Hammerstadt model for conductor roughness. Which one is correct? Both models are actually suitable for analysis of the 10.5 mil stripline on that board. However, if strips with substantially different widths are used, the model without roughness effect will be less accurate, assuming that all additional losses are due to conductor roughness. For instance if we use both models for analysis of 6-inch strip line with strip width 6 mil and 7.5 mil distance, two models will produce up

We Deliver...A 5-Star Performance

At U.S. Circuit, we are UL Certified to build **hybrid construction** with Rogers/FR408 family & Rogers/370HR as well as Isola I-Speed materials.

Call for a Quote: (760) 489-1413 or
email: rsojitra@uscircuit.com



U.S. CIRCUIT
Manufacturer of
Printed Circuit Boards

U. S. Circuit, Incorporated
2071 Wineridge Place
Escondido, CA 92029
Ph: (760) 489-1413
Fax: (760) 489-2965
www.uscircuit.com

Superior Quality
Superior Service

ITAR Registered

ISO 9001:2008

MIL-PRF-55110G

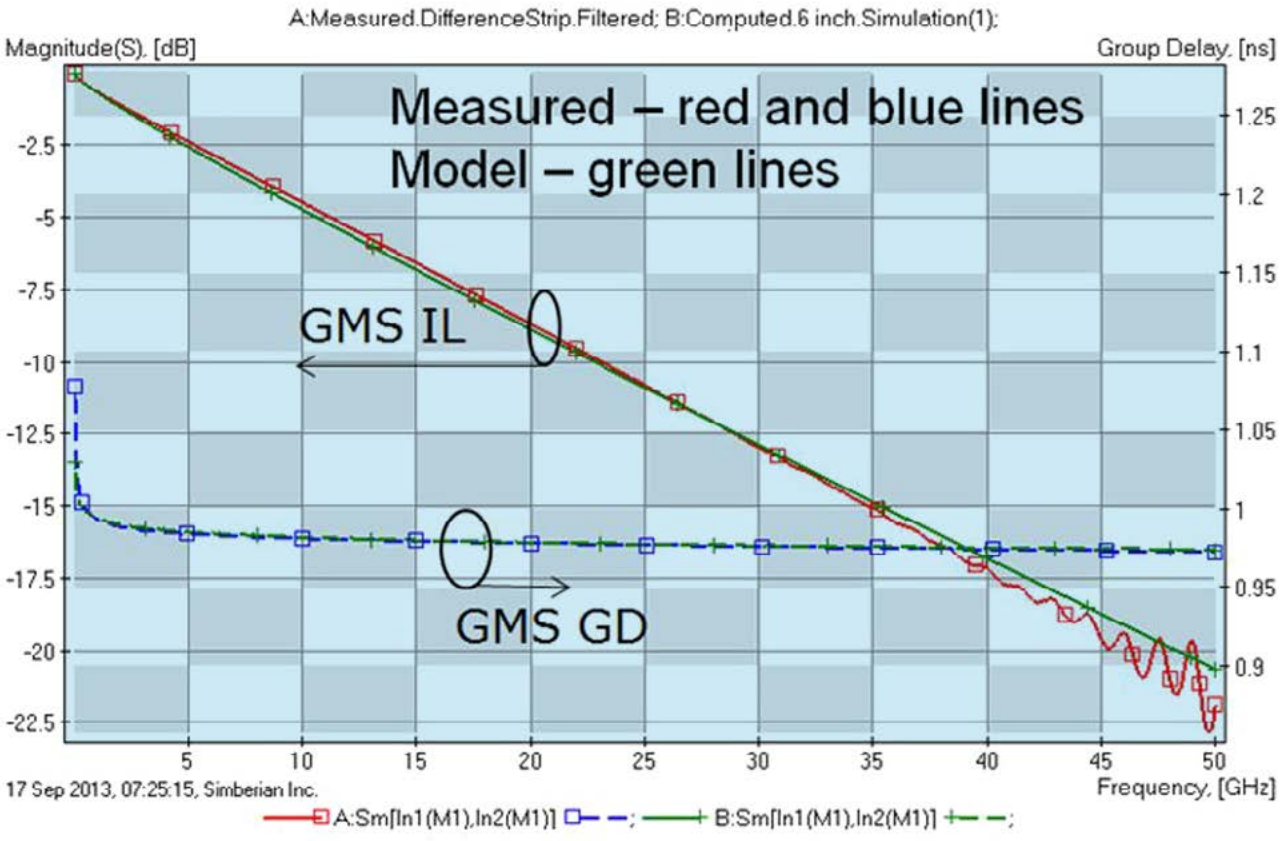


Figure 5: Measured (red and blue curves) and computed (green curves) GMS insertion loss (left plot) and group delay (right plot) for 6-inch stripline segments—wideband Debye dielectric model with Dk=3.83 (4.6% increase), LT=0.0138 (18% increase), smooth copper surface.

to 10% difference in the insertion loss as illustrated in Figure 7. Note that FR-408 can be considered as a medium-loss dielectric. Difference in insertion loss between model with increased LT and with proper roughness model can be as large as 30% starting from 3–5 GHz in cases of low-loss dielectrics[9] such as Megtron 6. Model with the rough conductor produces more accurate insertion loss estimation for broader range of strip widths.

This example illustrates typical situation and importance of the dielectric and conductor roughness model identification to have analysis to measurement correspondence up to 50 GHz.

Interesting results of dielectric and conductor roughness models identification with GMS-parameters for multiple materials were recently reported[10] and some data are provided in Table 1 as another practical example.

Note that all dielectric and conductor roughness models identified here are not actually restricted to the upper frequency 50 GHz level used in the identification process. The models are frequency-continuous and can be useful well above that frequency. This is one of the advantages of the broadband model identification method over approaches with resonators where dielectric properties are identified only at some frequency points.

Conclusion

An overview of frequency-continuous dielectric and conductor roughness models is provided in the paper. Such models must used in PCB and packaging interconnect analysis and measurement correlation up to 50 GHz and beyond. Practical procedure for the identification of the model parameters have been described

8 1/2 Reasons You WIN with Ventec

ventec

Show Me

PCB AND PACKAGING DESIGN UP TO 50 GHZ *continues*

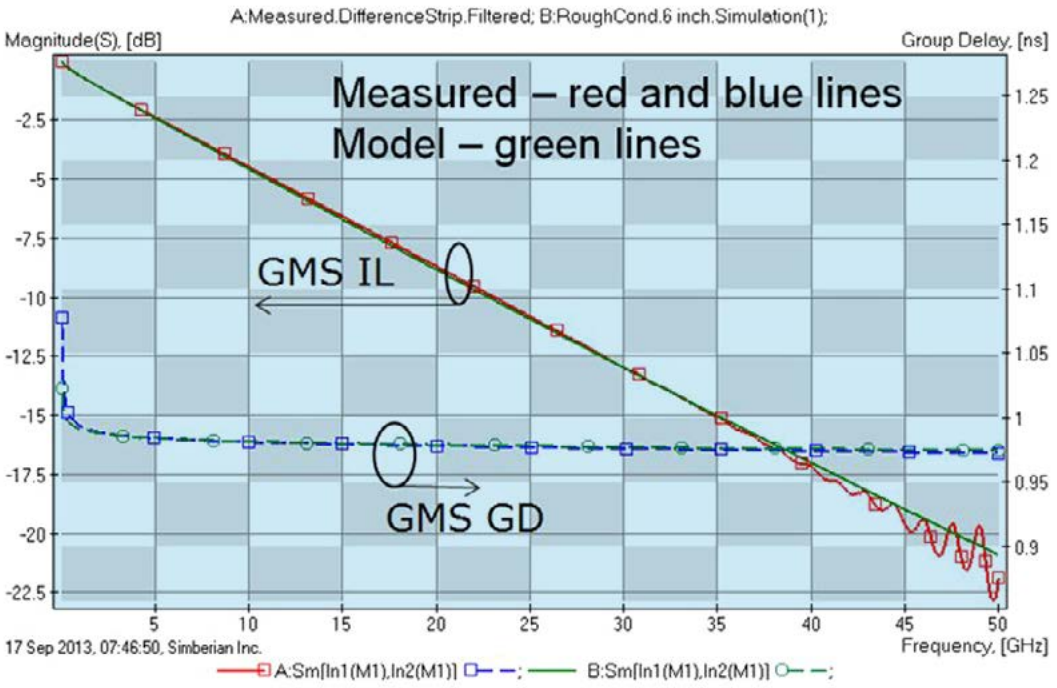


Figure 6: Measured (red and blue curves) and computed (green curves) GMS insertion loss (left plot) and group delay (right plot) for 6-inch stripline segments (Dk=3.8 (3.8% increase), LT=0.0117 (no change), Wideband Debye model, modified Hammerstadt model with SR=0.32 um, RF=3.3 for copper roughness).

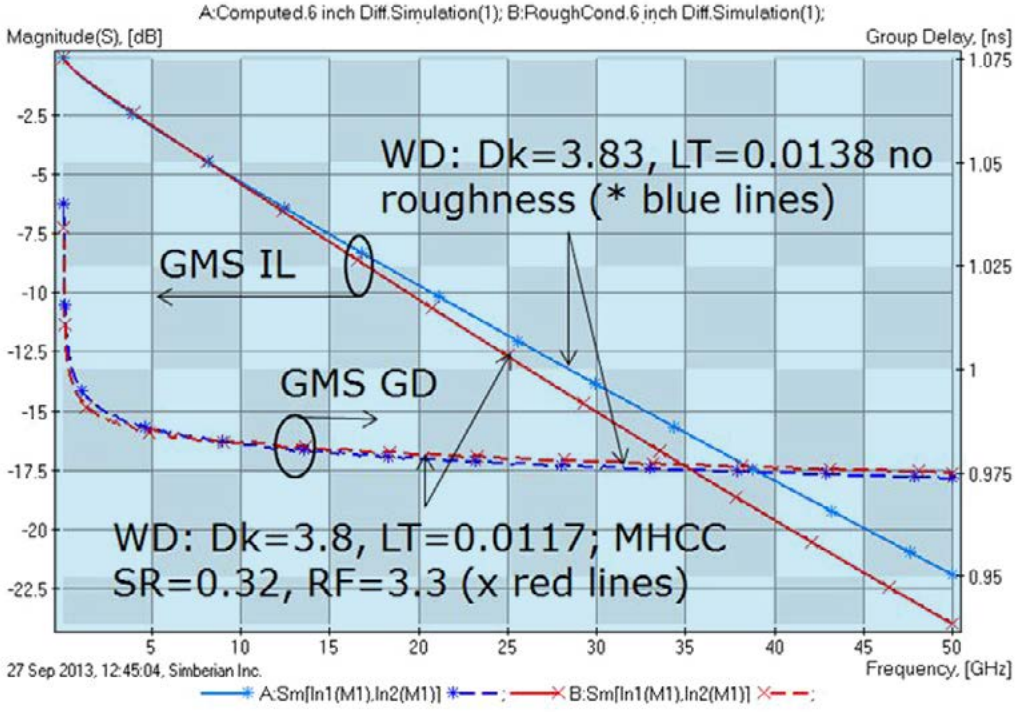


Figure 7: GMS insertion loss (left plot) and group delay (right plot) for 6 inch differential strip segments computed with roughness losses included into dielectric model (blue curves with *) and with separated conductor roughness model (red curves with x).

" Providing *Solutions* to Board Fabrication Challenges"

FROM CONCEPT TO COMPLETION

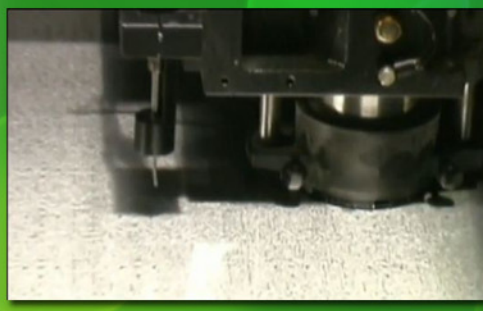
Solutions for Every Complex Situation

At Multilayer Technology we have the skills and the knowledge to be able to say "Yes We Can!" to your most complex design requirements.

We specialize in High-Speed Digital and RF Design constraints. In addition, we offer the following solution-based services:

- Extensive Exotic Material Processing
- Pre-DFM Services Available
- State-of-the-Art Industry Leading Processes
- Space-Based Reliability Requirements Standard

REQUEST A QUOTE



Multilayer Technology
3835 Conflans Rd
Irving, TX 75061-3914

(972) 790-0062

WWW.MULTILAYER.COM

ITAR

Mil-PRF-55110

AS 9100

Model Parameters / Board Types	WD Dielectric Constant @ 1 GHz	WD Loss Tangent @ 1 GHz	MH Roughness (SR, rms) (um)	MH Roughness Factor (RF)
Megtron-6 with HVLP copper	3.64 (3.6)	0.002	0.38	3.15
Megtron-6 with RTF copper	3.72 (3.6)	0.002	0.37	4
Nelco N4000-13EPSI with RTF copper	3.425 (3.4)	0.008	0.49	2.3

Table 1: Broadband material models identified in[10]. Dielectric constant and loss tangent values define Wideband Debye model (2), Dk values in brackets and loss tangent are from datasheets, roughness parameters are for modified Hammerstadt model (Eq. 4).

in details. It is shown that proper separation of loss and dispersion effects between dielectric and conductor models is very important. Without proper roughness model, dielectric models become dependent on the width of strips used in the test structures. If strip width is changed, difference in insertion loss predicted by models with roughness effect accounted in the dielectric models may be up to 20–30% off from the proper model with conductor roughness.

Note that PCB materials are composed of glass fiber and resin, and have layered structure and thus display anisotropy. Separate dielectric models for composite and resin layers may be required as shown in reference 10, or vertical and horizontal components of dielectric constant will have to be separately identified. Also, differences in dielectric properties of glass and resin can cause further signal degradation in form of skew and jitter induced by the fiberweave effect. Composite material models to account for all these effects are available in Simbeor software[8]. **PCBDESIGN**

References

1. Y. Shlepnev, Modeling frequency-dependent conductor losses and dispersion in serial data channel interconnects, Simberian App. Note #2007_02, www.simberian.com/AppNotes.php.

2. Y. Shlepnev, Modeling frequency-dependent dielectric loss and dispersion for multi-gigabit data channels (with experimental validation), Simberian App. Note #2008_06, www.simberian.com/AppNotes.php.

3. P. G. Huray, O. Oluwafemi, J. Loyer, E. Bogatin, X. Ye, Impact of Copper Surface Texture on Loss: A Model that Works, DesignCon 2010.

4. Y. Shlepnev, C. Nwachukwu, Roughness characterization for interconnect analysis. Proceedings of the 2011 IEEE International Symposium on Electromagnetic Compatibility, Long Beach, CA, USA, August, 2011, p. 518-523.

5. Y. Shlepnev, A. Neves, T. Dagostino, S. McMorrow, Practical identification of dispersive dielectric models with generalized modal S-parameters for analysis of interconnects in 6-100 Gb/s applications. DesignCon 2010.

6. Y. Shlepnev, System and method for identification of complex permittivity of transmission line dielectric, US Patent #8577632, Nov. 5, 2013, Provisional App. #61/296237 filed on Jan. 19, 2010.

7. Y. Shlepnev, System and method for identification of conductor surface roughness model for transmission lines, Patent Pending, App. #14/045,392 filed on Oct. 3, 2013.

8. Simbeor Electromagnetic Signal Integrity Software, www.simberian.com.

9. E. Bogatin, D. DeGroot, P. G. Huray, Y. Shlepnev, Which one is better? Comparing Options to Describe Frequency Dependent Losses, DesignCon2013, paper and presentation, www.simberian.com/AppNotes.php.

10. W. Beyene, Y. C. Hahm, J. Ren, D. Secker, D. Mullen, Y. Shlepnev, Lessons learned: How to Make Predictable PCB Interconnects for Data Rates of 50 Gbps and Beyond, DesignCon 2014.

Yuriy Shlepnev is the founder and president of Simberian Electromagnetic Solutions, a company that develops and distributes electromagnetic signal integrity software for the design of PCB and packaging interconnect.

I-Connect007 House Ad

Effective Routing of Multiple Loads

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

In a previous Beyond Design, Impedance Matching: Terminations, I discussed various termination strategies and concluded that a series terminator is best for high-speed transmission lines. Different terminating strategies have advantages and disadvantages depending on the application, but in general, series termination is excellent for point-to-point routes, one load per net. In summary, series termination reduces ringing and ground bounce.

But, what if there are a number of loads—how should these transmission lines be routed? For perfect transfer of energy and to eliminate reflections, the impedance of the source must equal the impedance of the trace(s) to the load.

Bifurcated transmission lines—traces that are split into two or more T-sections—are sometimes used to distribute signals to multiple loads. The impedance of the bifurcated line is not constant along the trace route, as the traces branching from the T-section are virtually in parallel when you consider the equivalent AC circuit. In this case, proper termination has not been provided and an impedance discontinuity can be seen at the branch point. In Figure 1, a 50 ohm signal from the driver is split into two transmission lines of 50 ohms and then into the loads. At branch (A), the two 50 ohm traces in parallel equate to a 25 ohm equivalent trace, and a mismatch in impedance. Figure 2 illustrates the resultant waveform of the unmatched transmission line.

Bifurcated transmission lines with matched impedances are a better choice. Rather than having the traces all the same width, the branch traces are reduced in order to match the impedance at the branch. The impedance of the traces after the branch then becomes 2 x Zo or 100

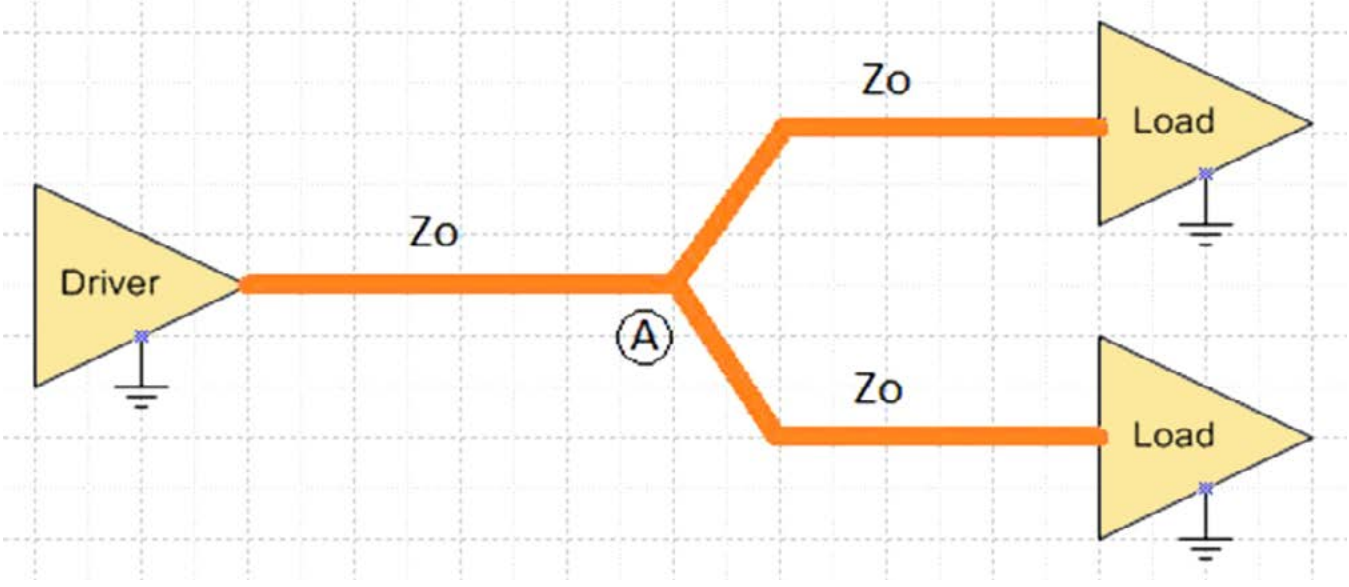


Figure 1: An unmatched bifurcated transmission line.

Our family is over 250 strong ...and growing.

We have more than 250 active customers, and we give each and every one industry-leading service and support. They are like family to us. In addition to delivering quality and reliability, we take the time to provide the service and support that makes each job a great experience for every member of our (growing) family.

Learn more about Dragon Circuits

Sounds great! Let's start a quote.

DRAGON CIRCUITS

Legendary manufacturing, service and engineering.

www.dragoncircuits.com | info@dragoncircuits.com | 972.790.7610

EFFECTIVE ROUTING OF MULTIPLE LOADS *continues*

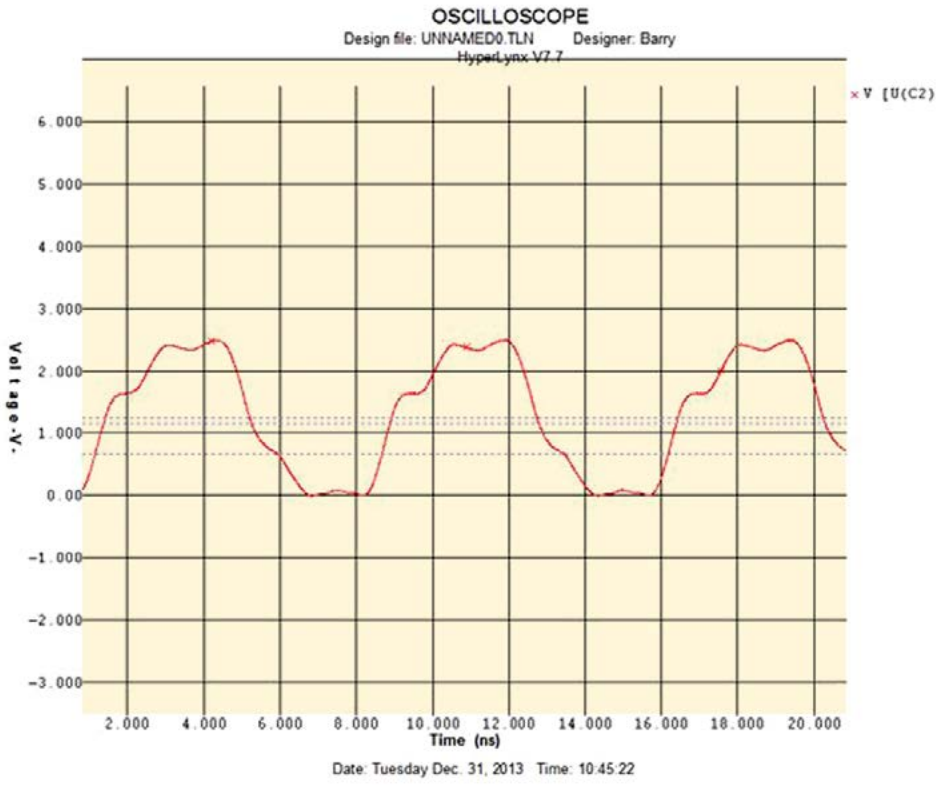


Figure 2: The resultant waveform of the unmatched line.

UNITS: mil — ICD STACKUP PLANNER FX – www.icd.com.au — 1/13/2014

Differential Pairs > 50/100 ohm

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)
		Soldermask		Dielectric	3.3	0.5					
1	8	Signal	Top	Conductive			1.4	12	24	1.15	51.89
		Prepreg		Dielectric	4.3	14					
2		Plane	GND	Conductive			1.4				
		Core		Dielectric	4.3	39					
3		Plane	VCC	Conductive			1.4				
		Prepreg		Dielectric	4.3	14					
4		Signal	Bottom	Conductive			1.4	12	4	0.31	104.69
		Soldermask		Dielectric	3.3	0.5					

Figure 3: The ICD Stackup Planner solves the impedance of 24 mil trace of 52 ohms compared to a 4 mil trace of 104 ohms.

ohms, and since these are in parallel the load seen at the branch is 50 ohms.

This would work fairly well if we could just halve the trace width. But, the width of the trace is not directly proportional to the impedance and a field solver is required to calculate the correct width required. For instance, a 24 mil trace of 52 ohms has to drop to 4 mil to double in impedance given the same substrate. This is solved by the ICD Stackup Planner Field Solver in Figure 3. The ICD Stackup Planner can be downloaded from www.icd.com.au.

This configuration also requires parallel pull-down resistors of 2 x Zo at each load. These end terminators ensure that the transmitted pulse progresses once down the line and then

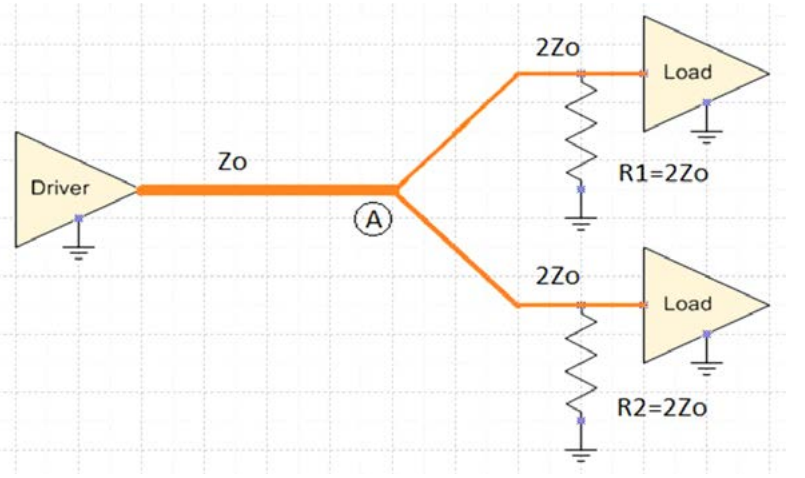


Figure 4: A matched bifurcated transmission line.

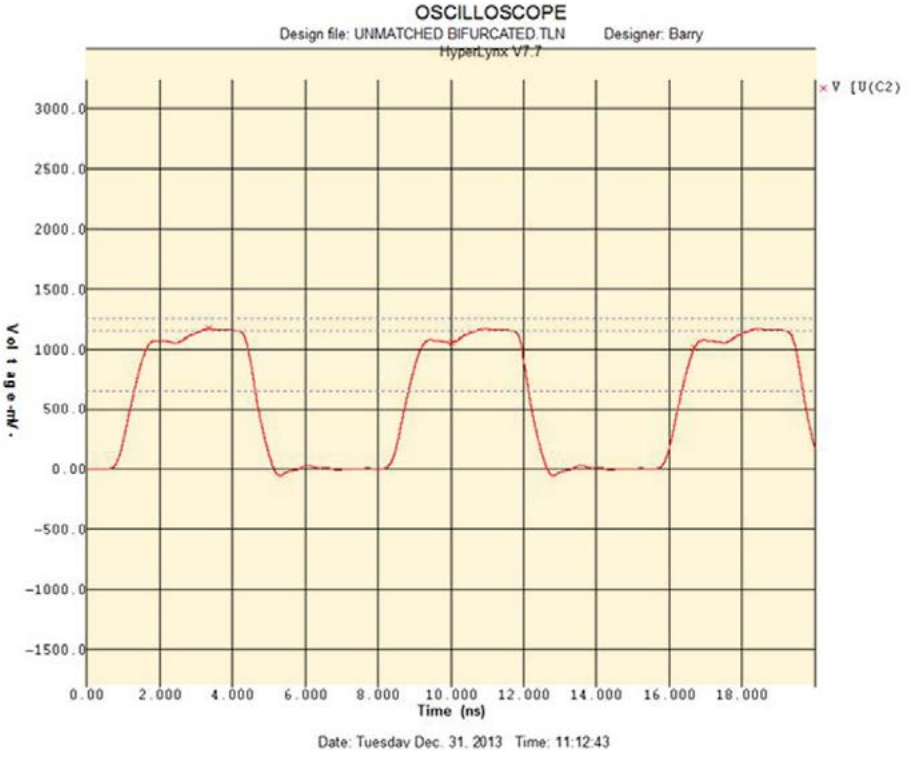


Figure 5: The resultant waveform of the matched line.

stops—preventing reflection—which is what impedance matching is all about.

Figure 5 illustrates the improved waveform of the matched bifurcated line of Figure 4. This technique, for matching branched lines, is not often used due to the difficulty of fabricating traces of widely varying impedance on the same substrate. Also, space limitations beneath FPGAs limit the width of the thicker trace. Another issue with this technique lies with the loop return currents created within the network. If one of the bifurcated traces is located on a different layer to the other, the return current will be referenced to different planes. When this occurs, a potentially large loop area is created, with a corresponding increase in radiated emissions. GND

EFFECTIVE ROUTING OF MULTIPLE LOADS *continues*

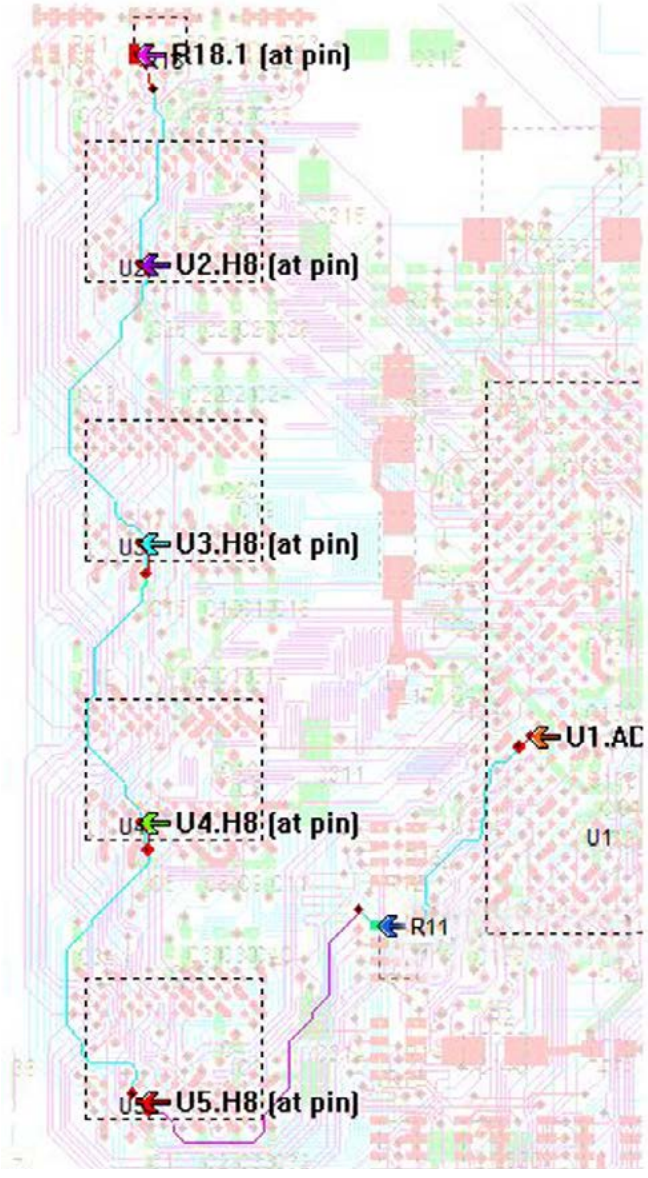


Figure 6: Multi-drop address routing.

stitching vias may help alleviate this problem.

We've covered differential clock and strobe routing in previous columns, but let's look at address routing. Fly-by topology—as used in double data rate design—uses a daisy-chain or multi-drop topology on address, command and control signals.

Fly-by topology reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew between the data and strobes at every chip/SDRAM requiring controllers to compensate for this skew by adjusting the timing per byte lane.

In this case, a series terminator (R11) is employed close to the driver and a parallel 100 ohm VTT pull-up (R18 resistor network) at the end of the loads. If the distance from the source to the first load is short, then the series terminator may not be required. But, this should be determined by simulation. The ideal location for end terminators is past the last load—with no side branch or stub—as depicted.

Stub length should be kept to a minimum. You can see how the address line, highlighted in Figure 6, is routed directly over the memory/load pin with a very short stub going off to each load. Since this stub is extremely short, compared to the transmission line length and length of the rising edge, an impedance mismatch is avoided. Short stubs, and their associated receiver capacitance, act like simple capacitive loads which tend to roll-off the rising edge.

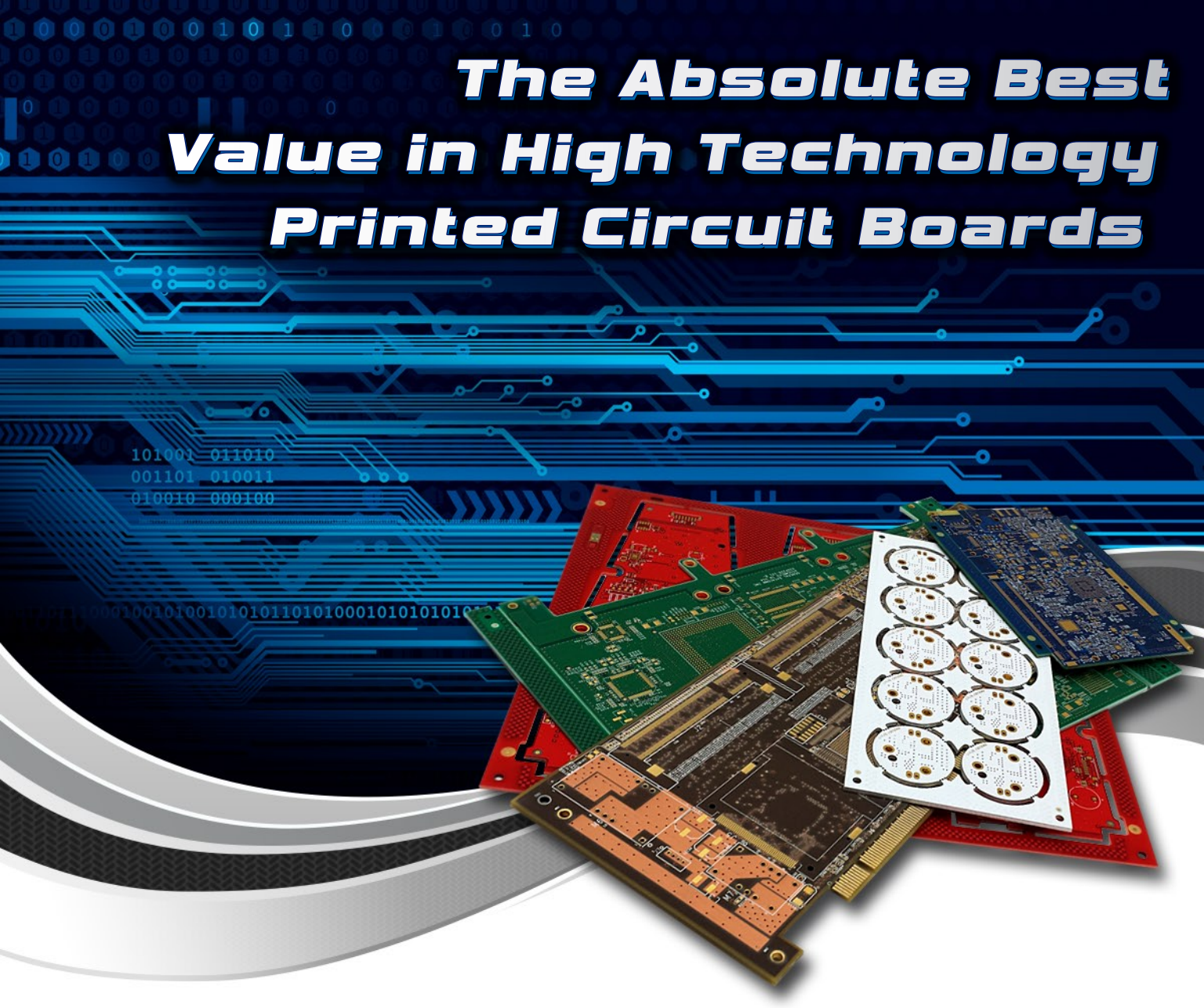
This configuration is ideal for DDR design but what if there is a slower rise-time clock that needs to be distributed to a number of loads?

Star routing is ideal for distributing clocks to multiple loads and is also used for power distribution on signal layers. The routing fans-out from a central point and connects to each load. But, with distributed loads also comes unmatched lengths between the loads. If a single series terminator is used, close to the source as in Figure 7, the different trace lengths cause different delays to each load which is unavoidable unless the lengths are matched. This also creates reflections which can be seen in Figure 8. Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance.

In Figure 9, three individual series terminators are used in conjunction with three different trace lengths. Figure 10 illustrates the resultant clean waveform.

If all the trace lengths, of the star configuration, are matched to length/delay then these reflections do not occur. So there is a choice: match the lengths or use individual series ter-

The Absolute Best Value in High Technology Printed Circuit Boards



Since 1971, Eagle Electronics Inc. has provided our Customers with the highest quality Printed Circuit Boards at fair and competitive prices. We are committed to exceeding our Customers' expectations and requirements, acheiving **total customer satisfaction** on each and every job. It's just the way we do business!

With Eagle, you can expect:

- Rapid Response to Quote Requests
- Fair and Competitive Pricing/Costs
- 100% Quality Performance
- 100% On-Time Delivery Performance
- Flexibility Scheduling
- Stock/Consigned Inventory Programs
- Thorough follow-up after job completion
- Total Satisfaction!

EAGLE electronics Inc.

MANUFACTURERS OF QUALITY PRINTED CIRCUIT BOARDS

click here for more reasons why you should use eagle!

www.eagle-elec.com

EFFECTIVE ROUTING OF MULTIPLE LOADS *continues*

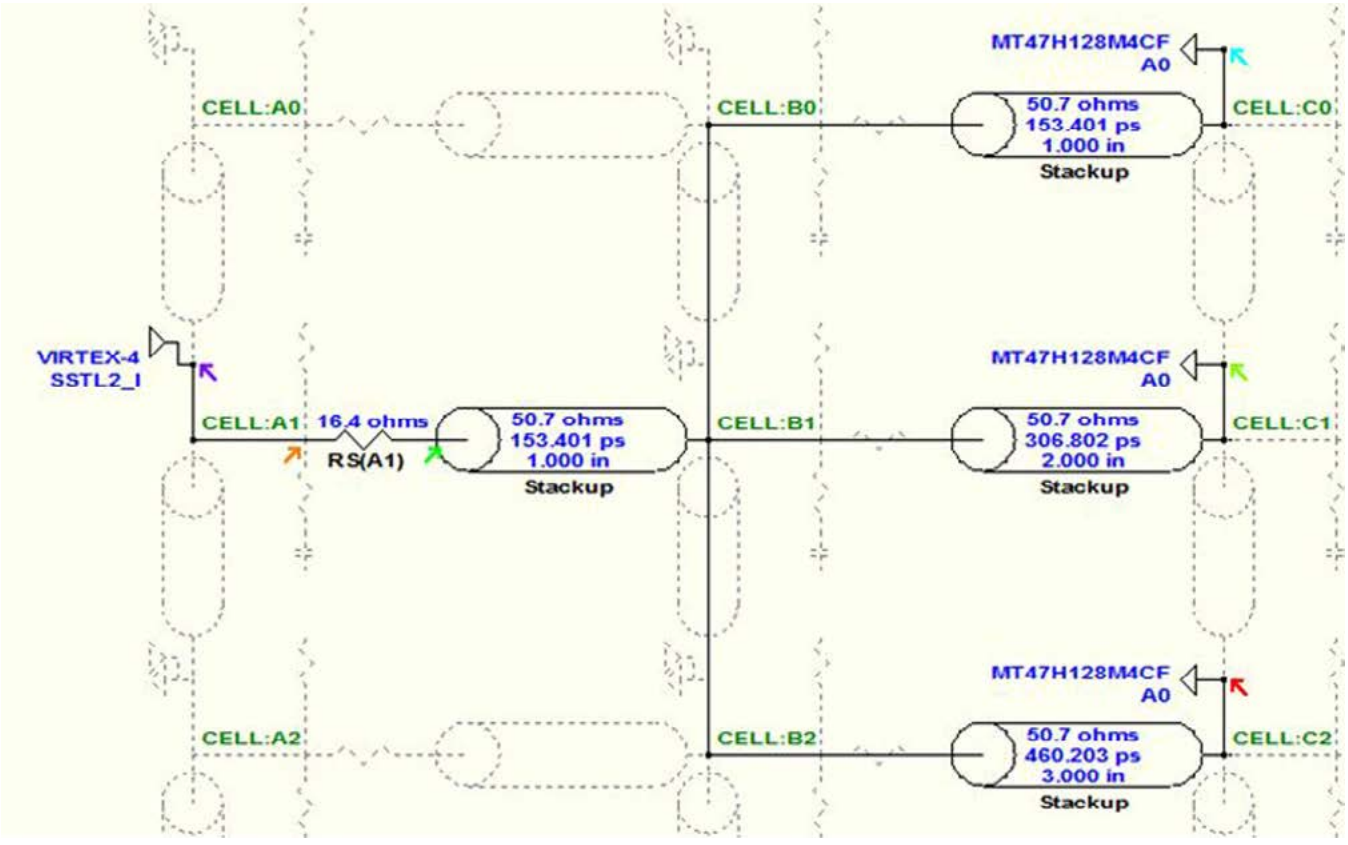


Figure 7: A single series terminator close to the source.

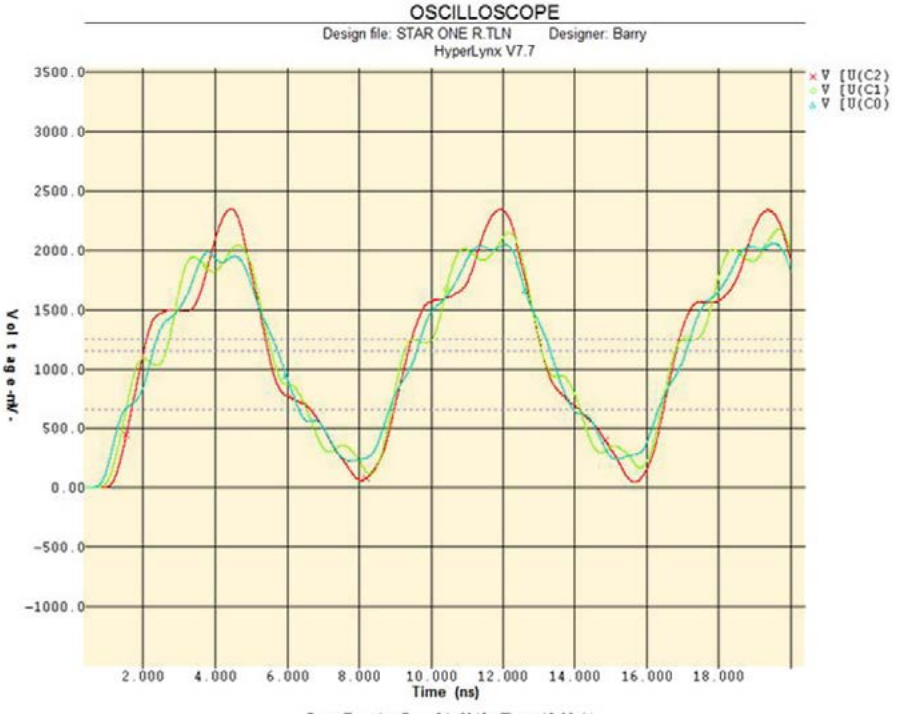


Figure 8: Reflections of the unmatched lines.

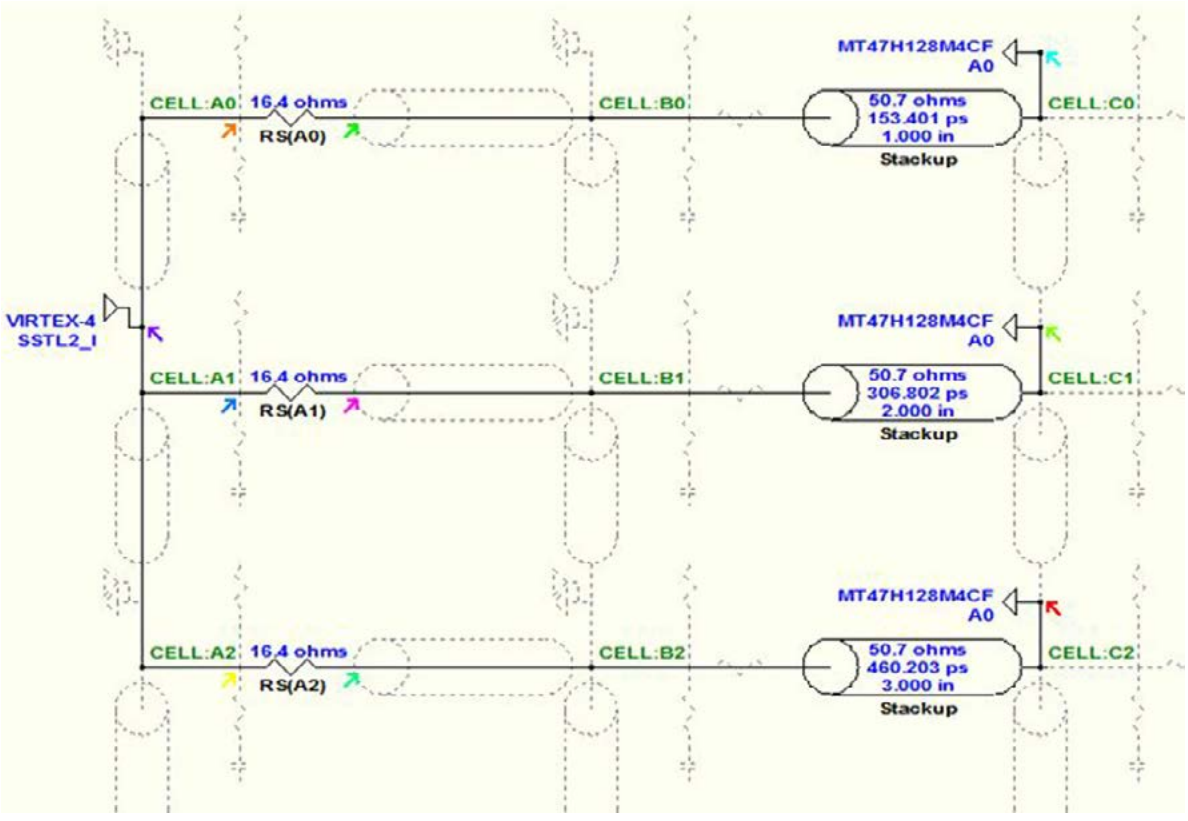


Figure 9: Individual series terminators at the source.

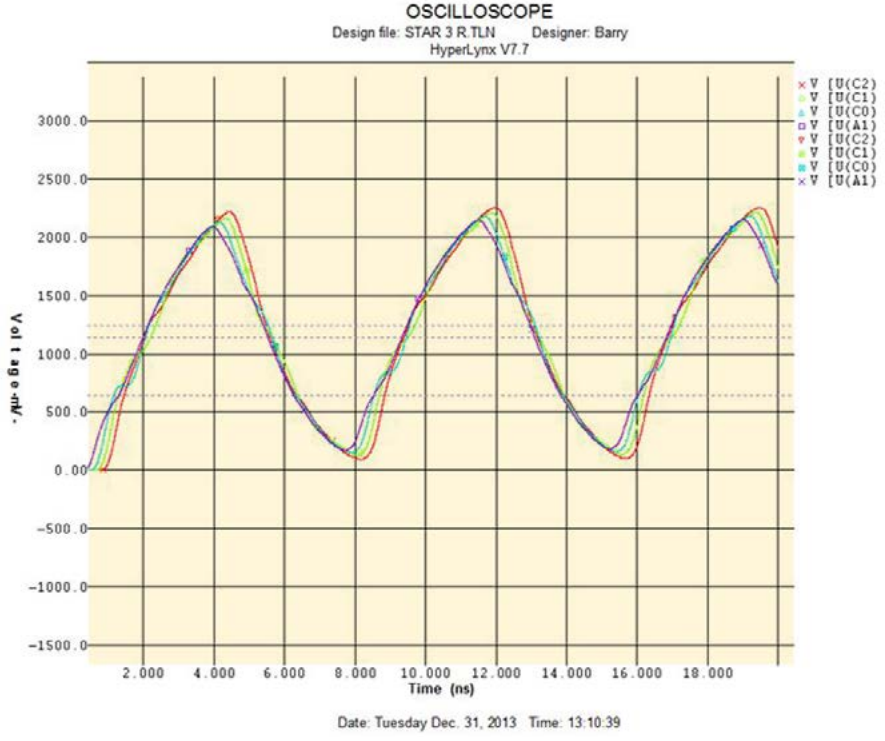


Figure 10: The resultant waveform of individual series terminators.

EFFECTIVE ROUTING OF MULTIPLE LOADS *continues*

minators close to the source to dampen the reflections.

Points to Remember

- A series terminator is best for high-speed transmission lines.
- Bifurcated transmission lines—traces that are split into two or more T-sections—are sometimes used to distribute signals to multiple loads.
- At the branch, the two 50 ohm traces in parallel equate to a 25 ohm equivalent trace—and a mismatch in impedance.
- Trace width is not directly proportional to impedance.
- Bifurcated transmission lines with matched impedances are a better choice.
- The end terminators ensure that the transmitted pulse progresses once down the line and then stops, preventing reflection.
- Matching branched lines are not often used due to the difficulty of fabricating traces of widely varying impedance on the same substrate.
- If one of the bifurcated traces is located on a different layer to the other, the return current will be referenced to different planes potentially creating a large loop area and EMI.
- Fly-by topology employs a series terminator close to the driver and a parallel 100 ohm VTT pull-up at the end of the loads.
- Star routing is ideal for distributing clocks to multiple loads and is also used for power distribution on signal layers.
- Reflections occur if the trace lengths of star routing are unmatched.
- The choice is this: Match the lengths or use individual series terminators, close to the source, to dampen the reflections of a star route.

PCBDESIGN

References

1. Barry Olney—Advanced Design for SMT, Beyond Design: Impedance Matching: Terminations,
Beyond Design: Differential Pair Routing, PCB Design Techniques for DDR, DDR2 & DDR3, Part 1,
PCB Design Techniques for DDR, DDR2 & DDR3, Part 2
2. Howard Johnson—High-Speed Digital Design
3. Mark Montrose—EMC and the Printed Circuit Board
4. The ICD Stackup Planner and PDN Planner—www.icd.com.au

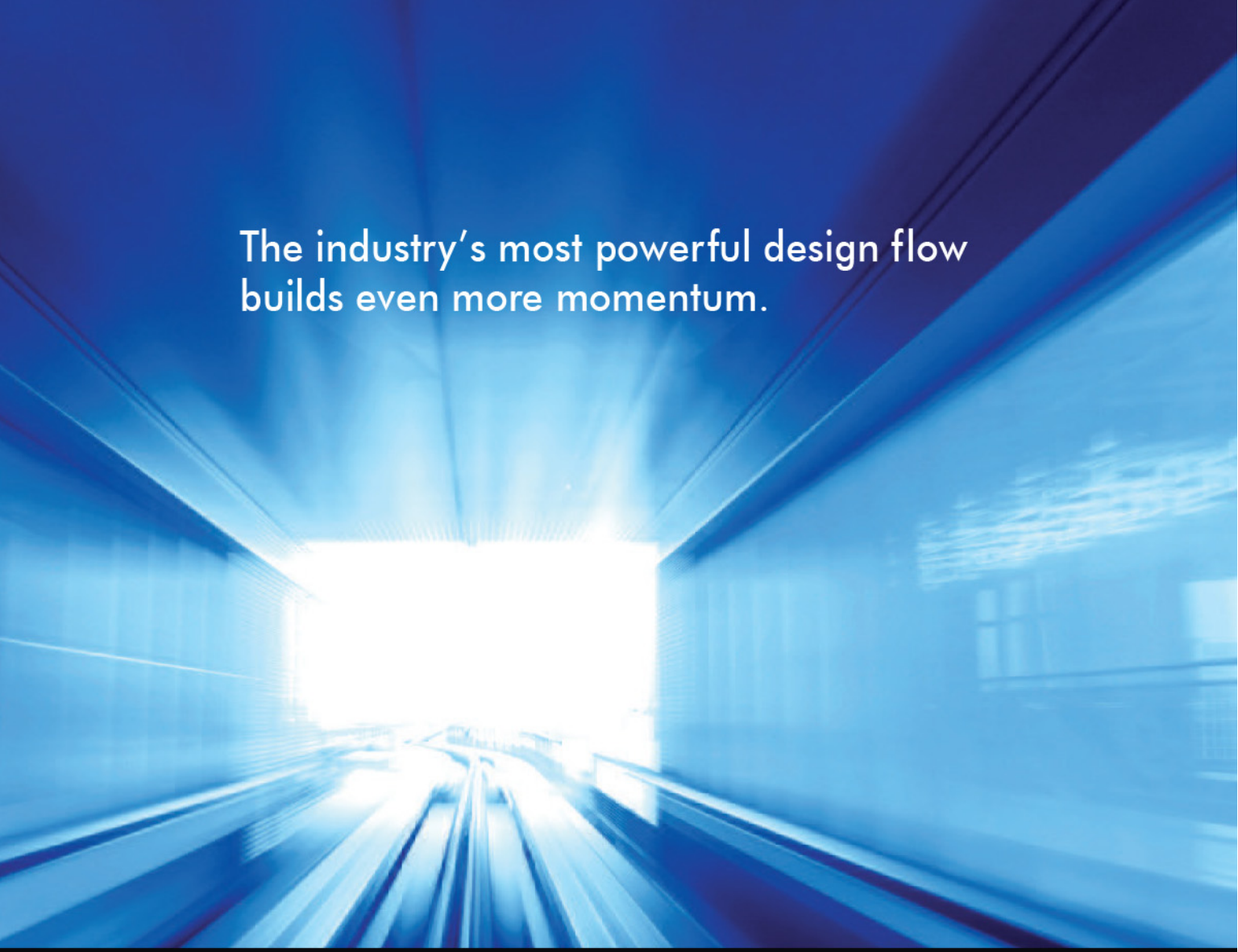
Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

Energy Harvesting Systems to Reach $375M by 2020

Energy harvesting systems offer an attractive alternative to battery power for portable devices. According to a recent report from Navigant Research, worldwide revenue from energy harvesting systems will grow from $283 million in 2014 to nearly $375 million in 2020.

Another important application for energy harvesting is pervasive sensor networks, where thousands of sensors monitor all measurable commodities, in real time. These devices diligently work to provide important information about temperature, humidity, security, machine health, structural health, and much more. As an alternative technology to power these networks, energy harvesting offers several advantages over conventional power supplies.

The report, "Energy Harvesting," analyzes existing and emerging energy harvesting technologies in depth, looking at nine end-use consumer and industrial application segments and the four most successful transduction methods for converting ambient energy. An Executive Summary of the report is available for free download here.



Our superior PCB, RF, and Hybrid design software guides you quickly and seamlessly from analysis to schematic to layout to manufacturing, with total design flexibility. Intercept's EDA environment solution includes powerful database translators for easy migration, full library support, advanced CAE/schematic design software, CAD/layout software, the industry's most powerful reuse block technology, and much more. Our customers achieve 100% manufacturability the first time.

PCB+HYBRID+RF DESIGN SOFTWARE, INCLUDING:
REUSE BLOCK TECHNOLOGY
MULTI-BOARD, PANEL ARRAYS
ARTWORK PANELIZATION
LAYOUT DRIVEN DESIGN & PROTOTYPING
INTERFACES TO SIMULATION & ANALYSIS
HIGH SPEED MATCHING, AUTO-TUNING
BIDIRECTIONAL RF INTERFACES
AUTOMATIC DRAWING CREATION
DESIGN AUTOMATION
DFM + MANUF. RULE CHECKING
ARTWORK VERIFICATION

pure engineering™
INTERCEPT

Please visit us at Apex in booth #1847

www.intercept.com

PCB007 News Highlights

IPC: PCB Sales Improving Despite Weaker Orders

"While sales continued to strengthen in the North American PCB industry compared to last year, orders declined," said Sharon Starr, IPC's director of market research. "This disparity between sales and order growth pushed the book-to-bill ratio to its lowest point since March 2009," she added, "indicating a slow and possibly bumpy recovery going into 2014."

Spirit Circuits Acquires Lyncolec

After six months of negotiation, innovative PCB manufacturer Spirit Circuits is pleased to announce the acquisition of Poole, UK-based PCB manufacturer Lyncolec. The company is well-known for supplying rigid, flex, and hybrid multilayer PCBs.

IPC Redefines Microvias, Again

In 2013, IPC changed its definition of a microvia. Before then, a microvia was defined as any printed board with holes that have a diameter of equal to or less than 0.15 mm [0.006 in]. Over time, that size became common, while more challenging geometries emerged to alter the definition of microvia structures.

IPC's 2013: A Year in Review

Within the printed board fabrication arena, IPC released updates to two of its most popular flexible circuit standards: IPC-6013C, Qualification and Performance Specification for Flexible Printed Boards, and IPC-4203A, Cover Bonding Material for Flexible Printed Circuitry.

PCB Solutions Doubled PCB Engineering Projects in 2013

PCB Solutions is pleased to announce yet another year of excellent growth in one of its core services: Engineering design and PCB layout. The company developed engineering services most of the 2013 year and made great strides in growing its engineering division.

Innovative Circuits Doubles Capacity with Drill Acquisitions

"These new drills allow us to use all of our drills more efficiently," says Russell Nolan, manager of drill and route operations. "This acquisition speeds up our operations tremendously and increases our ability to meet our customers' quick-turn demands."

Murrietta Circuits Achieves ISO-13485 Certification

Albert Murrietta, COO and co-owner, announces that his company has achieved full ISO-13485 registration for the medical marketplace. Murrietta is now one of the few companies in the nation that can offer a true full turnkey solution, from design through final assembly, with complete medical ISO registration.

MFLEX Doubles Sales to New Customers

Reza Meshgin, CEO, commented, "Net sales to our newer customers more than doubled sequentially, and are expected to represent approximately 23% of total net sales. Looking ahead to the fiscal second quarter, we expect a significant sequential decline in net sales that we anticipate could approach 40%."

AT&S Named ZTE's Best Quality Performance Supplier

On December 12, 2013 ZTE held an awards ceremony for Excellent Suppliers. In addition to winning the "Excellent Delivery" Award in 2012, AT&S was awarded the "ZTE Annual Best Quality Performance Award 2013" as core supplier.

Impact of Inexpensive Flex PCBs on Cell Phone Production

Using flex circuits as the interconnect choice in the assembly of cell phones will bring huge benefits. These boards have low mass and cause cell phones to be much lighter. They are capable of housing small conductors with high wiring density, taking up less space. Being lighter and smaller will result in an end-product that is more versatile.

DESIGN. FABRICATION. ASSEMBLY. TEST.
ALL UNDER ONE ROOF.

We are a full turnkey shop that brings every part of the process together. Our one-company **integrated** solution results in better quality for your job and less hassle for you. One purchase order results in one complete product!

Murrietta Circuits
The Integrated Solution

MIL-PRF-5510

ITAR

sales@murrietta.com | **www.murrietta.com** | (714) 970-2430

Understanding the Typical CAM Process

by Mark Thompson CID+
PROTOTRON CIRCUITS

Editor's Note: This column also appears in this month's issue of The PCB Magazine.

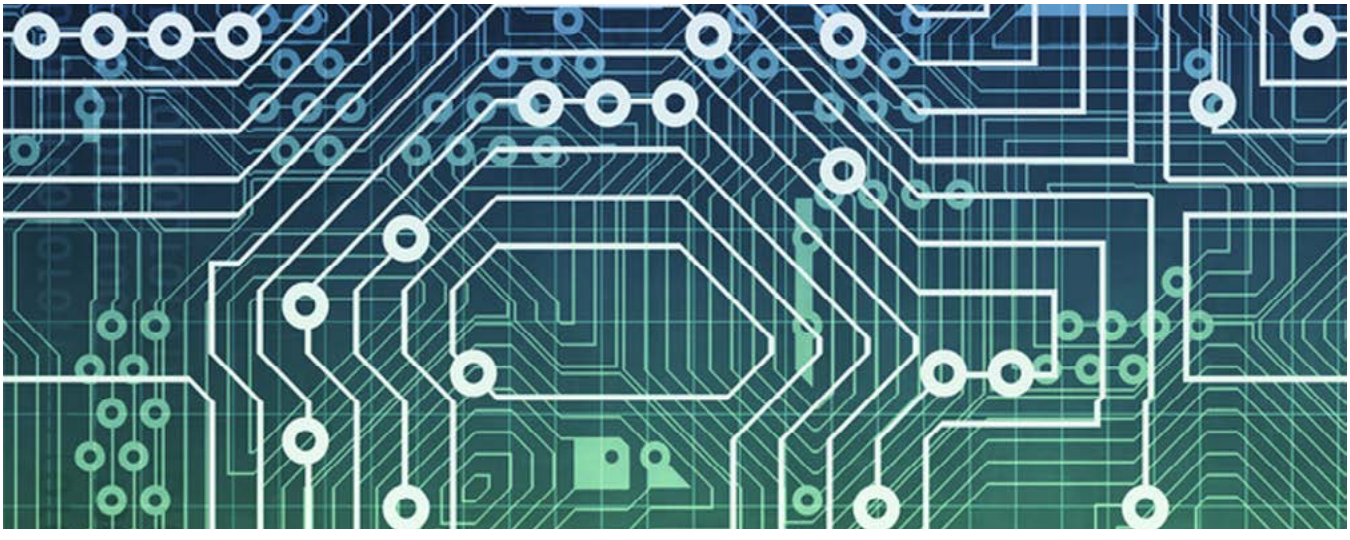
CAM vs. Capability

Many new customers have some misconceptions about what a typical fab shop can and cannot do. There are levels of manufacturing that need to be well understood by the buyer. The PCB buyer needs to know where a board will be a good fit based on the parts' complexity. How does this happen? How does the PCB buyer or a contract manufacturer know who is (or is not) a good fit based on a myriad of different designs, from simple 2–4 layer RF parts to high-layer count HDI, blind and buried via parts? If the part is of medium complexity, it can be built by virtually any mid to higher level PCB fabricator. Many times it boils down to things like quote response time. More diligent buyers may use a tool such as The PCB List where they can compare technology levels side-by-side and make good decisions about where a part should go. Not all PCB buyers need a shop that can do 2 mil lines and spaces or laser stacked vias. Sometimes the product dictates a shop of this type must be used; other times, when a given design does not "push" the fabricator's limits, more fabricators obviously have an opportunity to show what they can do.

What is CAM?

Not all board fabricators have the ability to have both CAD and CAM. You may say to yourself, "But a CAM tool should be able to do some, if not all, CAD functions." And that is true. But if you are really getting to the design level, you need to have a design team. Many PCB fabricators do not have design capabilities but do have the ability to understand the customers' needs and recognize design attributes.

Let me give you some examples of this, ranging from simple CAM assumptions to more complex ones. Let's say a design has copper poured right to the edge of the part, but is NOT a Z-axis or edge-plated part. A good CAM department may do a very minimal clip of the metal around the periphery like .003–.004". This is imperceptible to the end-user as it appears metal is right to the edge and if the metal would have been left alone there may be burring at final rout (functional, but not cosmetically the best). Again, this is where a good CAM person comes into play: When would they NOT do something like a minimal clip for rout? An example



Mentor Graphics®

GET YOUR PRODUCTS TO MARKET FASTER

When it comes to looking for a competitive advantage,
your PCB design strategy can ultimately prove to be your secret weapon
as you move into an uncertain future.

Are you providing your design teams
with access to the right technology to make that happen?

Speed time-to-market today
with the PCB technology of tomorrow

LET US SHOW YOU HOW

VIRTUAL PROTOTYPING

DESIGN FLOW CONCURRENCY

DESIGN THROUGH MANUFACTURING

Follow us

See us in Vegas!
APEX EXPO IPC Booth #616

UNDERSTANDING THE TYPICAL CAM PROCESS *continues*

would be RF launches on an obvious RF part; here, we know the intention is to literally have metal right to the edge and that any burring at final rout is acceptable with the customer. This is where their understanding of electrical function comes into play, along with years of practical experience.

And when I say CAM department, I mean both people and tools, as the tools are only as good as the people behind them. I have said many times that a good CAM operator is worth his weight in gold.

Likewise there are many levels of designers and layout folks, some with years of knowledge and good common-sense layout practices. These are the guys and gals that ask the important questions at the right time, which is to say at the design/layout stage and not after the PCB gets to the board fabricator.

> ***Sometimes CAM is a compromise between pad size, drilled hole size, copper weight and available space. Don't rope yourself into anything if you don't have to. If the hole is a legitimate via and you really don't care about its finished hole size make it +.003" minus the entire hole size.***

What Does a Fabricator do with Your Data?

To start, let's go through what a board fabricator needs from an output CAD package briefly and talk about what edits are done at the manufacturing stage and why you need to know about them.

Regarding output packages, what does a fabricator need to be able to fab your part?

1. Image data of all the layers involved including mask files, silkscreens and pastes exported as either Gerber 274D, 274X, or ODB++. At least one of these files should have a part outline on it, unless you are providing a drawing with a dimensioned hole or feature.
2. NC drill file or files (for blind or buried). Typically, Excellon 1 or Excellon 2 format.
3. An IPC-356 type netlist so the fabricator can run the design against the exported Gerber.
4. A drill drawing with hole sizes, dimensions and drill symbols chart.

If the part is impedance controlled, the drawing should describe what lines are being controlled, where they reside and what threshold and tolerance they need to perform at.

Now the fabricator has the job. Will my data undergo any modifications for manufacturing? Yes, so let's go through them.

1. Drill compensation for plated holes, slots or edge features

Depending upon surface finish, fabricators will drill anywhere between .004" and .005" over your specified finished hole size (FHS) to plate back down to your nominal size. Since this is something done by all manufacturers your output data should have already taken this into account. Fabricators like to see a minimum of .002" per side annular ring pad to hole after this drill compensation on signal layers and at least .005–.006" per side pad to copper pour after the drill compensation.

Sometimes CAM is a compromise between pad size, drilled hole size, copper weight and available space. Don't rope yourself into anything if you don't have to. If the hole is a legitimate via and you really don't care about its finished hole size make it +.003" minus the entire hole size. This tolerance tells the fabricator it is okay to drill smaller to deal with things like annular ring minimums and can mean the difference between a quote from a fabricator and a "no bid."

2. Etch compensations for image data

Depending upon the starting copper, all image data is compensated at the CAM stage to account for the known loss at the fabricators etcher. Typical rule of thumb is a half-mil of additional line or metal feature width for every half ounce of starting copper.

Exception to this rule is quarter oz copper foil where no etch compensation needs to be added. Quarter-ounce foils are typically only used for outer or surface layers.

Again, your design should be able to accommodate these compensations. Example: If your design is .003"/.003" and you are asking for 2 oz. copper you will get a phone call from your fabricator.

3. Panelization

If you are ordering parts as an array either as a tab rout, score or combination of both you will want to provide a sub panel drawing with any particulars your assembler may need like additional tooling, fiducials, specific areas where not to place a tab due to part overhang issues at assembly, etc.

If you have no preferences and your chosen assembler does not need anything special typically the board fabricator can come up with a good sub panel that works well for both manufacturing and assembly. For instance: Even if no tooling or fiducials are specified for the given array, many times fabricators will add them to the array anyway. They are generally of no harm at that point and can be quite helpful if tooling and fiducials were not foreseen.

4. A 1-up compare and net-list compare

The fabricator will perform a 1-up compare at the CAM stage even if no IPC netlist is provided. This is to ensure the addition of the drill and etch compensations does not create manufacturing capability violations. A 1-up compare is only that; it is not a netlist compare. If an IPC-356 file is provided, the fabricator will also run the provided IPC netlist against your provided exported Gerber data. Remember this is a design vs. exported Gerber file comparison. If you do not provide an IPC netlist for a class 36012 job, your fabricator will ask for one. I have been asked many times over the years to simply generate a net-list based on their exported Gerber data. If a netlist is generated by the fabricator based on the Gerber data, at what point would we ever find a mismatch? So what is my point? If you would like us to verify your design iteration against your exported Gerber data please provide an IPC netlist.

A brief note about IPC net-lists and their generation: Avoid creating test points for things that will be connected only after the devices are loaded, such as surface mounts or edge-plated castellations. This will avoid a phone call from your fabricator with false or erroneous "broken" or open nets. Likewise, many times in a design an AGND to DGND short is designed in and is intentional. Make note of these intentional net-list anomalies.

Throughout this article I have used the term "artwork" but today you have fabricators that can send the image data from CAM directly to a direct image device, eliminating the use of films and thus another transgression of the artwork image. Every copy you make loses a little in the translation. If you can image the cores and outer layers directly, this loss is minimized.

Common Fabrication CAM Issues

1. RF parts

RF type applications typically require a specific design tool suite that does not always deal with things like RF impedance controlled traces in a conventional manner. For example:

RF traces are often drawn as a composite of many smaller line sizes to be able to deal with the unique shapes and reflections needed for RF work. This is a nightmare for a CAM operator. The size being controlled may be specified as .025", but when the CAM operator queries the apertures used for .025", they do not exist. Again, this is because they have been drawn as a conglomerate or composite of many smaller trace widths.

2. Same size trace width for single-ended impedance structures, differential pairs and copper pour

This does not allow the CAM operator to easily select one or the other for any unique re-sizing that may be necessary for meeting or getting closer to the customers' desired impedances.

For years, I have advocated using a tenth or a hundredth of a mil to differentiate between single-ended traces, diff pairs and copper pour that are using the same draw size. Fabricators cannot resolve this small difference but it allows the CAM operator to select and deal with those structures without affecting the others. I am happy to see this is becoming the norm.

UNDERSTANDING THE TYPICAL CAM PROCESS *continues*

3. Etch and drill compensations not taken into account at the design and layout stage

This can mean the difference between a quote and a "no bid" from a fabricator.

Do not make the pads only .005" over the finished hole size or you will get a phone call from your fabricator, as this does not allow for drill compensation plus a minimum of .002" per side annular ring pad/hole. The same goes for slots or other edge-plated features.

Additionally, make sure the design allows for etch compensations based on the copper weight you are specifying. Again the rule of thumb is half mil for every half-ounce of starting copper. Specific information about etch and drill compensations can be gleaned from the fabricator as different shops require different process minimums. Add to that, if your design needs to meet IPC, these things should have already been factored into the design.

Drawings and Data Don't Match

Sometimes this happens due to rounding errors from metric to imperial or vice versa, but sometimes it happens because the part has been revised and the note is no longer applicable. Remember to review the drawings to make sure all information contained is valid and/or still required.

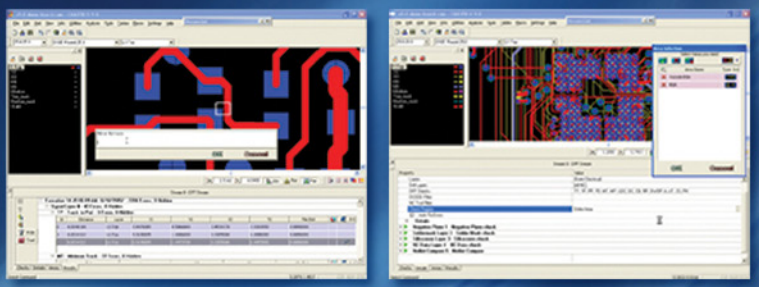
These are but a few examples of things a CAM department will run into. I hope this has helped you understand a small part of the CAM process as it relates to board fabrication. Feel free to send me your feedback! **PCBDESIGN**

Mark Thompson is in engineering support at Prototron Circuits. To read past columns, or to contact Thompson, click here, or phone 425-823-7000, ext. 239.

Solutions to Ensure PCB Manufacturing Success!

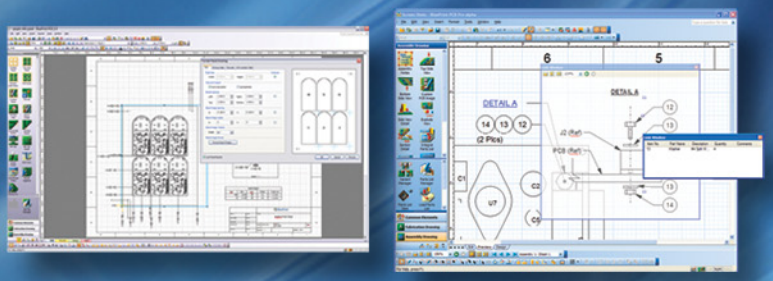
CAM350®

Verify and Optimize PCB Designs for Successful Manufacturing.



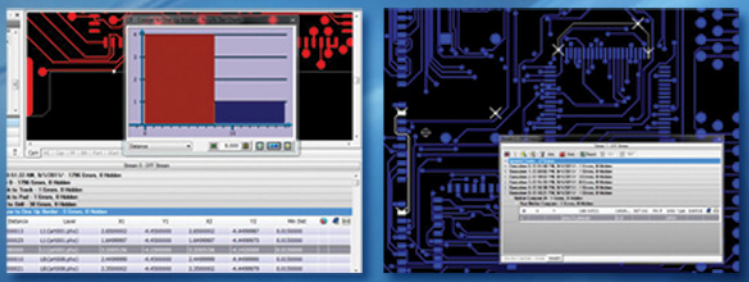
BluePrint·PCB

Create comprehensive documentation to drive PCB fabrication, assembly and inspection.



DFMStream™

Verify Design and Manufacturing Rules Any Time During the PCB Design Cycle.



At DownStream Technologies we are committed to delivering comprehensive solutions and workflow process improvements for all your PCB post processing needs.

For more information please visit downstreamtech.com or call 800-535-3226.

DownStream Technologies

What's Driving High-Speed PCB Design?

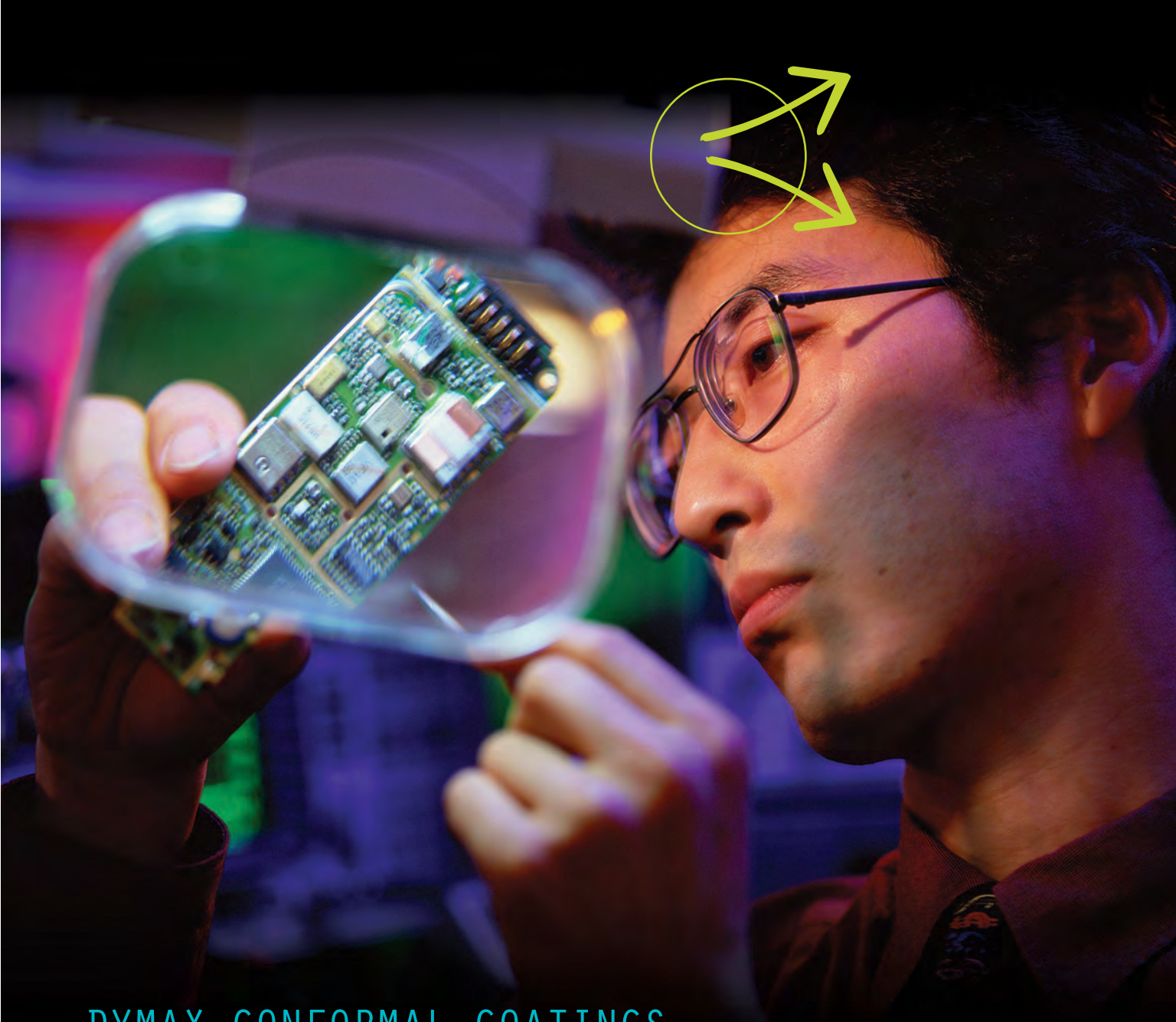
by Amit Bahl
SIERRA CIRCUITS

Advances in semiconductor manufacturing have paced the development of electronics for six decades. The smallest transistor geometries are one thousandth the size possible 40 years ago, and that scaling, along with innovations in materials and architecture, has resulted not only in the integration of whole systems on chips, but device speeds that now challenge the limits of carrying digital signals over copper traces on FR-4 for distances as long as a desktop computer motherboard.

I venture that progress in electronics now hinges not so much on semiconductor advances as it does on a transition to PCB laminates that have better dielectric properties than FR-4. Consider the latest USB chip sets. A consortium of semiconductor, PC, and software companies drafted the original Universal Serial Bus standard in the 1990s to provide a common interface for connecting all sorts of peripherals to personal computers, one that could support the disk-drive data rates at the time and also supply power to external equipment. That standard specified two communication modes: a "full-speed" mode with a 12-Mb/s maximum signaling rate and a low-speed mode for such devices as a keyboard or joystick. The USB topology consists of a central host residing in a PC, and multiple ports downstream of that host controller, which can connect with peripherals that may in turn serve as hubs for communication with other equipment.

The original standard was amended within a few years by USB 2.0, which upped the maximum signaling rate by 40 times to 480 Mb/s. That version was superseded in 2008 by USB 3.0, which increased the maximum rate to 5 Gb/s. USB 3.0 is backward-compatible with the preceding standard, but includes a new high-speed bus in parallel with the USB 2.0 bus. In 2013, the standard was again upgraded, adding an even faster transfer mode whose ceiling is 10 Gb/s. The first chip sets to support the latest version of the standard, USB 3.1, will be introduced this year.

A peripheral that would communicate in the fastest mode can be connected to the host by a cable up to a meter long. The total allowable



DYMAX CONFORMAL COATINGS. BETTER PROTECTION AND HIGHER THROUGHPUT. BEYOND A SHADOW OF A DOUBT.

Dymax Conformal Coatings cure in seconds with UV light – and with ambient moisture curing available for shadowed areas, you can be confident you're getting maximum protection – even underneath components. Add vivid blue fluorescing for easy inspection of coating coverage, and you'll see more throughput, in less time, using less floor space. All with unsurpassed protection against moisture, dust, chemicals, and temperature cycling. And, they're backed by the Dymax Edge… an integrated offering of oligomers, customized adhesives and coatings, cure and dispense equipment, and application expertise that enables Dymax to deliver the best solution to the customer. Visit **dymax.com/conformalcoating** to download the new *Guide to Light-Cure Conformal Coatings*.

877-396-2988

DYMAX®

DYMAX.COM

WHAT'S DRIVING HIGH-SPEED PCB DESIGN? *continues*

loss in the channel end-to-end through the external device to the host controller is -20 dB at the maximum signaling rate, according to the model by the USB organization. The channel model includes loss from the cable, loss from the connectors, loss in the device PCB, and at most a 7-dB loss across the host PCB, based on a 10-inch maximum trace length there. Active repeaters would be required if loss exceeds that -7 dB budget. Of course, the rescue to compensate for the signal degradation through the channel is equalization, both on the transmit and receive sides.

Microchip, one of the companies that manufactures chip sets to implement USB 3.0 (5-Gb/s maximum signaling rate), points out in their implementation guidelines:

> ***Eventually, the expense of developing tricks to skirt the limitations of conventional PCB materials won't be cost-effective, and the slight premium for a material with far less loss will be well worth the price. I submit that we're close to that threshold.***

Signal losses for copper traces running on FR-4 materials can be very significant at USB 3.0 SuperSpeed (SS) signaling rates. Ways to mitigate losses include:

1. Keep SS traces as short as practical. This is the single most practical and cost-effective thing that can be done to reduce signal loss.
2. Route SS traces on outer layers, rather than on inner layers.
3. Consider laminates with lower DF and DK ratings. These lower-loss materials include FR408HR, FR408HRIS, N4000-13SI, Rogers.
4. Try to route SS signals at a 45-degree angle to the material weave direction so that the trace does not occasionally line up with a high-resin, high-loss path.
5. Consider low-loss materials, like N4000-13SI or Rogers.

Note they twice emphasize switching from FR-4 to low-loss materials, and this is in an application note for devices to implement 5-Gb/s communication, not the upcoming chips to enable double that rate.

Jim Choate, the USB technology product manager at Agilent Technologies, recently presented a webinar about compliance testing for USB 3.1 devices. He started his career working on computer motherboard design and validation at Intel during the 1990s and later served as the USB Implementers' Forum (USB-IF) compliance committee chairman. He contends there is enough margin to push USB signal rates beyond 10 Gb/s without abandoning FR-4 for PC motherboards, but concedes repeaters would be necessary and very likely much different architectural approaches for USB chip sets. From his experience at Intel, he believes that using a material other than FR-4 for a PC motherboard would be a deal-breaker.

Who would wager that each future generation of semiconductor devices, whatever their function, won't be faster than their predecessors? Eventually, the expense of developing tricks to skirt the limitations of conventional PCB materials won't be cost-effective, and the slight premium for a material with far less loss will be well worth the price. I submit that we're close to that threshold.

There's nothing intrinsically expensive about the constituents and manufacture of many high-performance materials, except for the special SiO2 glass in some products. Naturally, while the demand for such materials is low, their price will remain a little higher than that of materials in high demand.

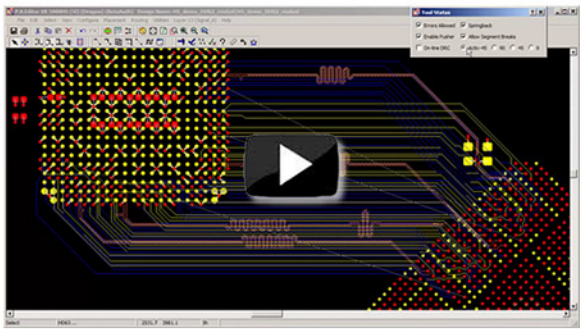
Would 30% lower loss at 10 GHz be worth it to you? **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by clicking here.

ZUKEN™

Cut your PCB design time

Step up to CADSTAR - Start your trial today



Advanced 45-degree routing and pushing

The ultimate in speed and precision for manual routing, the **Activ-45** router provides single-click "follow me" routing with automatic completion, using push-aside, springback and segment break options to tackle even the most complex layout challenges.

Be a "Smart designer" - Download the CADSTAR App

CADSTAR Touch is a free PCB design productivity App that allows remote control of CADSTAR's view and program functions.

- Pan
- Zoom
- View all
- Run Macros
- More...

Download on the App Store

GET IT ON Google play

CADSTAR includes:

- Schematics
- Constraint Browser
- Placement Planner
- High-speed routing
- Signal Integrity
- Power Integrity
- EMC
- 3D Mechanical verification.

CADSTAR™

CADSTAR - Proven expert desktop PCB design solution

www.zuken.com/cadstar-trial

Westford, MA, USA

Tel: 888 332 7227

Mil/Aero007 News Highlights

DfR Solutions Alliance Intensifies Government/Military Focus

"We are excited about the relationship with Circuit Solutions. Historically, DfR Solutions has successfully supported many government and military electronics reliability programs through SeaPort-e, NASA Safety and Mission Assurance Services, OSD Corrosion Prevention and other programs," said Craig Hillman, CEO of DfR Solutions.

3D Printing Coming to Military Applications

As researchers at Picatinny Arsenal explore the potential of three-dimensional printing, they envision the possibility of embedding a radio antenna on the side of a soldier's helmet or printing sensors directly onto a weapon or even an article of clothing.

Total Market for Electric UAVs to Top $1B by 2023

The total market value for electric unmanned aerial vehicles will reach over one billion dollars by 2023 according to findings in the new IDTechEx report, "Electric Unmanned Aerial Vehicles (UAV) 2013-2023."

Global Electronic Warfare Market to Reach $12.15B in 2014

The global electronic warfare market is estimated to be $12.15 billion in 2014 and is expected to register a CAGR of 4.50% to reach $15.59 billion by 2020.

Report Outlines Declines in Defense Spending

The decline of defense spending will likely force new revenue streams for the aerospace and defense industry that may include innovations in intelligence, precision strike technologies, and cyber security. "It is anticipated that global revenues for the defense sector will track to similar levels as in the past two years, particularly in the U.S. and Europe," said Tom Captain, DTTL Global Aerospace and Defense Sector leader.

Global Dimensional Metrology Market in Aerospace Industry

New analysis from Frost & Sullivan, Assessment of the Global Dimensional Metrology Market in the Aerospace Industry, finds that the market earned revenue of $482.9 million in 2012 and estimates this to reach $592.1 million in 2017. The research covers CMM, measurement gages, vision measuring machines, as well as optical digitizers and scanners.

Thermal Imaging Market to See CAGR of 10.9% 2013-2018

The thermal imaging market is estimated to grow from $3.49 billion in 2013 to $5.84 billion in 2018. This represents a compound annual growth rate (CAGR) of 10.9% from 2013 to 2018.

Port Security Market to Hit $36.99 Billion by 2018

The global port security market is being driven by the increasing need for sustaining business continuity, threats on ports, and government initiatives. Security of the ports is extremely important to attract both domestic and international investors.

APAC Maritime Issues Impact U.S. Military Needs

The recent U.S. strategic pivot toward the Pacific has placed that region at the forefront of change in the military. Where in the recent past activities in the area of responsibility for the U.S. Central Command defined military needs, now the requirements for the U.S. Pacific Command are emerging as the leading edge of the defense technology sword.

U.S. ISR Video Analytics Budget to Decline

According to new research from Frost & Sullivan's U.S. ISR Video Analytics, the defense budget for this market will reduce to $837.5 million in 2018 from $1,207.2 million in 2012, as the combat operations in Afghanistan cease.

We are Commited to Delivering Outstanding Quality and Service, On-Time.

AND OUR CUSTOMERS AGREE!

Prototron Team,

Technology Kitchen develops microcontroller solutions for customers in many industries. Prototypes are a key piece to our phased development process.

We have appreciated the timely responses to our requests for quotes for various quantity, delivery and board finish scenarios. The Prototron team always hits the delivery date with quality boards! We have also appreciated your willingness to drop ship to various Technology Kitchen partners.

Everyone we interact with at Prototron makes Technology Kitchen feel like we are your only customer!

Thanks,

Ken Ward, Technology Kitchen

Click to Learn More

Prototron Circuits

Quality printed circuit boards

Visit us in Vegas!

APEX EXPO IPC *Booth #1463*

FASTEST

America's Board Shop

www.prototron.com

FAQ: Microwave PCB Materials

by John Coonrod
ROGERS CORPORATION

The landscape of specialty materials changes so quickly that it can be hard for product developers to keep up. As a result, PCB designers are inundated with data about microwave PCB materials. But very often, it's difficult to find useful information regarding these specialty substrates. So, this month, we present some of the most frequently asked questions about microwave materials encountered at Rogers.

Q: At what frequency is it necessary to transition from FR-4 types of materials to high-frequency circuit materials?

A: This is a challenging question to answer because different technologies can tolerate more or less performance from a laminate. I'll give a few examples and basic guidelines.

Semiconductor technology has developed enhanced signal processing to the point where a FR-4 material could be used at higher speeds and frequencies than was once thought possible. In most cases where high-speed digital applications reach 10 Gbps or more, you will need to use a high-frequency laminate. There are exceptions, and in some cases a lower data rate PCB will also demand a high-frequency laminate.

High-frequency RF circuits, which are less concerned with insertion loss, could use FR-4 in some of these applications. However, high-frequency laminates offer more than just low loss; they provide very well-controlled dielectric constant. In many RF applications, the control of dielectric constant for the material can be as critical as substrate thickness control. As a general statement, FR-4 materials are typically not used above 3 GHz in RF applications due to insertion loss concerns. However, when dielectric constant control is a critical concern, high-frequency materials should be used instead of FR-4 materials.

Auto Routing

OrCAD is Trusted by The Top 10 Automotive Manufacturers

Why? Because today's technology packed automobiles need an industry-proven, highly reliable, and seamlessly integrated electronics design solution. Cadence® OrCAD® PCB Design tools provide the complete, rules-driven design and analysis environment necessary to meet the demands of the automotive industry. Drivers trust their automotive electronics, electronics designers trust OrCAD.

Click here to learn more about OrCAD

cadence®

EMA Design Automation®

FAQ: MICROWAVE PCB MATERIALS *continues*

Q: Can high-frequency circuit materials be mixed with FR-4 materials for hybrid multilayer PCBs?

A: Yes, this is often done, and there are fewer compatibility issues than one may assume. A multilayer hybrid PCB using many layers of FR-4 and a few layers of high-frequency circuit materials is commonly utilized for several different reasons. In some cases, the reason is cost-related; the more expensive high-frequency laminates are used only in the layers where better electrical performance is needed.

In other cases, a mix of materials may be used for improved reliability. Some PTFE-based laminates have high coefficient of thermal expansion (CTE), which can be a concern when a circuit is built with many layers of this material. Hybrid multilayers have been built with very thermally stable FR-4 (with a low CTE) used on non-electrically critical layers to help offset the higher CTE of some PTFE laminates. As a side note, not all PTFE laminates have a high CTE and many with ceramic fillers have extremely good and low CTE values.

Another case is when it is necessary for a multilayer PCB to use materials of significantly different dielectric constant. In those cases, different high-frequency materials may be mixed together to achieve the goal. With many hybrid builds, the materials are often compatible, however special circuit fabrication processing is necessary. The material suppliers and circuit fabricators should always be involved when hybrid builds are required.

“With many hybrid builds, the materials are often compatible, however special circuit fabrication processing is necessary. The material suppliers and circuit fabricators should always be involved when hybrid builds are required.”

Q: Are high-frequency circuit materials more difficult to fabricate than standard FR-4 materials?

A: Like so many questions and answers in the engineering world, the answer to this question is “it depends.” There are several different types of materials used for high-frequency applications. The two most common circuit materials used are PTFE-based (such as DuPont’s Teflon) and filled hydrocarbon. Both of these categories have subcategories and the following gives some distinction as it relates to circuit fabrication.

PTFE materials that are unfilled or nearly pure PTFE are typically more problematic for the PCB fabricator, because it’s a soft material with a high CTE, and there are dimensional stability issues and special plated through-hole (PTH) processing challenges. PTFE laminates that are reinforced with woven glass negate many of the problems with softness, handling, and dimensional stability. When a laminate is a filled PTFE substrate, the CTE can be significantly improved, and the PTH preparation process is more forgiving. For ease of fabrication, the recommended material is a woven glass-reinforced ceramic-filled PTFE laminate. This laminate offers extremely good electrical performance and can be relatively friendly for PCB fabrication.

The different versions of filled hydrocarbon laminates can vary quite a bit, but in general they can be processed in the same processes as a FR-4 laminate. However, different parameters will be necessary for these processes, but usually the same equipment can be used. A few differences worth mentioning include the need for different speeds/feeds at drill, potentially less drill life, different parameters for PTH preparation using plasma or permanganate, and lamination parameters which are often very different from FR-4 prepreg.

Q: Why does the high-frequency industry need laminates with so many different dielectric constant options?

A: The need for different dielectric constant relates more to RF applications than digital ap-

SHAX Engineering

Delivering peace of mind to the industry since 1998.

hp

LOCKHEED MARTIN

maxim integrated™

GENERAL DYNAMICS

intel

cadence

These are just some of the major corporations that have placed their trust in us.

SATISFACTION GUARANTEED 100% SATISFACTION GUARANTEED

VIEW SHAX SERVICES

PCB Design. Fabrication. Assembly.

www.shax-eng.com | 800.814.3680

FAQ: MICROWAVE PCB MATERIALS *continues*

plications. In the microwave range of frequencies (about 300 MHz to 30 GHz), the PCB circuit patterns are often the microwave circuit component. As an example, a bandpass filter might not be a component that is soldered onto the PCB, but is actually the conductor pattern of the PCB. An edge-coupled series of conductors and space can act as a bandpass filter at microwave frequencies. A simple microstrip edge-coupled filter is shown in Figure 1 and its function is based on wavelength which is related to the dielectric constant of the material.

Wavelength is a property of an electromagnetic wave that propagates on the circuit. As the name implies, the wavelength is the physical length of the wave and this length is dependent on the dielectric constant of the material and the frequency. The size of many microwave components is based on a fraction of the wavelength; often ½ or ¼ wavelength is used to define circuit features.

In Figure 1, there are line segments with small spaces between them. It may be hard to believe but electrical energy will pass through this circuit very effectively, at the right frequency. The length of each pair of conductors (with a space between them) is ¼ the wavelength at the intended frequency. With conductor lengths at ¼ of the wavelength, there will be a lot of electric energy radiated on one of these elements and that energy couples to its neighboring element (line segment). At the right frequency, the energy of the propagating wave will jump from one element to another, going down this circuit. However, when energy is introduced into this circuit pattern at a different frequency, the wavelength will be different and the energy will not couple from one element to another. Therefore, no electrical energy will propagate.

The physical size of this bandpass filter is related to wavelength at the frequency of interest. If the circuit material dielectric constant is much higher, the size of the circuit would shrink in order to maintain the same wavelength properties. Having a high dielectric constant material can reduce the size of a microwave circuit. This is only one example of many, but in general, microwave circuitry is very dependent on the dielectric constant of the material because the technology uses wavelength properties to produce many different types of circuit functions. Wavelength is very much related to dielectric constant, and a higher dielectric constant yields shorter wavelength.

Q: Why is insertion loss getting so much attention on new applications?

A: Actually, the microwave industry has been concerned with insertion loss for decades. However, now more digital applications are focusing on this concept. Insertion loss is a complicated subject, so I can only give a simple overview here. But in general, insertion loss is the total electrical loss of a high-frequency/high-speed circuit.

Insertion loss is made up of a combination of many losses and one of them is dielectric loss. Usually dielectric loss is related to the dissipation factor (tan-delta, loss tangent) of the circuit material. As the name implies, dielectric loss is the property of a circuit where losses occur due to the substrate. Conductor losses are

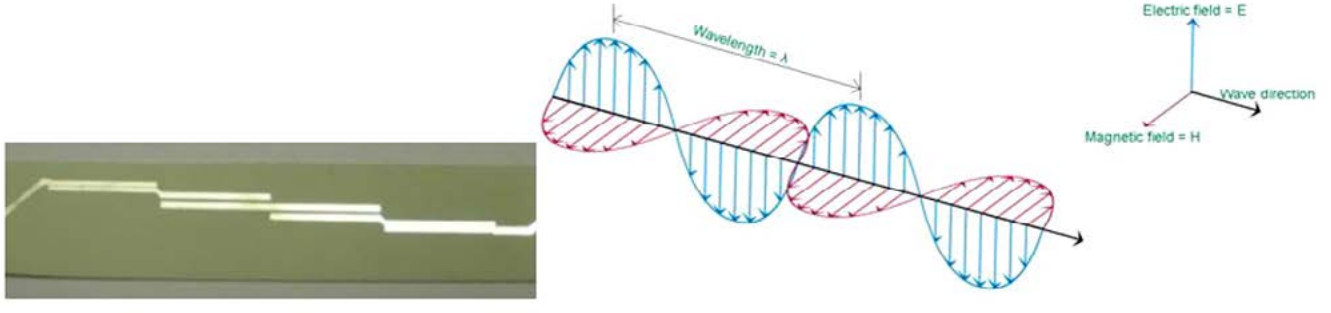


Figure 1. Microstrip edge-coupled bandpass filter as part of the PCB pattern, and a wavelength illustration.

APEX EXPO® IPC

CONFERENCE & EXHIBITION › March 25-27, 2014
MEETINGS & EDUCATION › March 23-27, 2014
MANDALAY BAY RESORT AND CONVENTION CENTER
LAS VEGAS, NEVADA
WWW.IPCAPEXEXPO.ORG

Design-Focused Education

March 21–24, 2014

NEW IDEAS...FOR NEW HORIZONS

› **DESIGN FORUM** — Educational program featuring presentations by experts in design, including:

- New Elements of IPC Design Programs
- Real Version Control: Gateway to Effective Data Management and Design Collaboration
- Enabling I/O Optimization with 3-D SoC, SiP and PCB Co-Design
- Enabling Efficient, Collaborative Design with IPC-2581

and more

› **PROFESSIONAL DEVELOPMENT COURSES** — Three-hour classes led by subject-matter experts, including

- DFX Design For Excellence - Design for Manufacturing, Design for Reliability, Design for Assembly – Parts I and II (PD-10 and PD-18)
- Making the Most of Design Time (PD11)
- Noise Control in High Speed Boards (PD14)
- Fundamental Considerations to EMC and High Speed Signal Behavior on PCBs (PD 26)

and more

› **DESIGNER CERTIFICATION PROGRAM** — Basic (CID) and advanced (CID+)

For more information on design-focused education,
visit **WWW.IPCAPEXEXPO.ORG/DESIGN.**

DESIGN | PRINTED BOARDS | ELECTRONICS ASSEMBLY | TEST

FAQ: MICROWAVE PCB MATERIALS *continues*

also part of insertion loss. This is loss that is associated with the copper conductors and finish. There is no perfect conductor, but copper is very good for conductivity. If another metal is added to the copper, the overall conductivity will typically decrease which causes more loss. The different finishes used in the PCB industry are typically lower in conductivity than copper and more loss occurs when some plated metal finish is added to the copper conductor. Also, the surface roughness of the copper conductor can cause more loss with a rougher (high-profile) copper surface. Conductor losses are frequency-dependent due to skin depth, and at some frequencies, the conductor losses are minimal while other frequencies can be significant.

Thermal management issues can be a concern when insertion loss causes the circuit to heat up when RF power is applied. A circuit with lower insertion loss will heat less with applied power. In the case of high-speed digital applications, insertion loss will cause the digital pulse to decrease in amplitude and cause possible distortion. Having a circuit with low insertion loss will allow the digital signal to maintain the good integrity needed.

There are many potential interactions between PCB fabrication, circuit design and material properties which need to be understood to ensure the finished circuit will meet the needs of the end user. It is always recommended to consult the circuit material's manufacturer for new designs and applications to ensure the optimum material is used for the application. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation's Advance Circuit Materials Division. To contact Coonrod, click here.

thepcblist

THE best way to find a PCB fabricator, anywhere.

Holaday Circuits Inc.

Minnetonka, Minnesota, U.S.A.

Website | Contact Me | RFQ

Overview | Contact | Specs | About | Videos | Photos | Brochures | News

Holaday Circuits has been producing quality Printed Circuit Boards for over 40 years. Our dedicated staff, state of the art equipment and technical expertise work together to meet the common goal of exceeding our customer's expectations.

Markets: Communication, Industrial, Medical, Military/Aerospace, Other: Downhole

Board Types: Multilayer, Other: HDI Technology, RF boards, Edge Plating, Copper filled uVias, Impedance, Sequential Lamination

Mfg Volumes: Prototype, Small, Medium, Other: DFM and Stack-up Analysis

Other Services: Quick turn-around

Specialities: Blind/buried vias, Bonded hea nks, Controlled depth drilling, Controlled Impe Filled/plugged vias, HDI, Laser a Sequential lamination

S-9100, IPC-6012 class 3, ISO 9001, gistered, MIL-PRF-31032, MIL-PRF-55 DCAP, ROHS compliant, UL

Click to see a partial list of registered OEMs!

Click here to see a demo

Why YOU should Showcase:

- Capabilities listing for advanced search functionality
- Specialties and certifications listing
- Ability to upload brochures and videos
- Quick and easy “Contact” and “RFQ” buttons
- News, web and contact links

www.thepcblist.com

TOP TEN

News Highlights from PCBDesign007 this Month

① View Full Coverage of DesignCon 2014

DesignCon 2014 is in the record books, but if you couldn't make the show, don't worry—we have full video coverage of this essential Silicon Valley engineering event. From the leading-edge technical conference to the packed exposition, our Real Time with... program brings it all to you.

② Mentor Announces GENIVI 5.0

Mentor has announced the availability of the latest release of its Mentor Embedded Automotive Technology Platform for Linux-based in-vehicle infotainment system development. Automotive Tier One suppliers can speed the development of rich and responsive user interfaces, similar to those seen in consumer electronics devices, with the new graphics development and optimization functionality added to this GENIVI 5.0 compliant release.

③ Zuken Innovation World 2014 Series Kicks Off in India

Zuken has expanded its annual Zuken Innovation World conferences following the success of previous years' events. This year's theme is "Power of Innovation," which has already inspired the speakers from companies around the globe.

④ Polar Instruments Joins HDP User Group

CEO Martyn Gaudion said, "We are very excited to participate in the HDP User Group. We will be active participants in the high-frequency test measurement project furthering the scope of the industry interface standard to better enable an open interface architecture between CAD and CAM tools."

5 Intercept, Moss Bay EDA Launch Low-cost EMC Solution

EMSAT now has several options for user flows from any layout software environment by utilizing Intercept's numerous database translators. EMSAT customers can use a DSN file output to analyze a layout for EMC or SI errors. Pantheon reads the error file from EMSAT, then displays the list of errors in a custom EMSAT Viewer dialog for real-time viewing.

6 PCB CAD Segment Down Slightly in Q3

The EDA Consortium Market Statistics Service reports that PCB and multichip module design software revenue dropped 0.3% YOY in Q3 2013. PCB/MCM revenue totaled $152.5 million in Q3 2013. The four-quarters moving average for PCB/MCM increased 7.6%.

7 EPTAC Unveils IPC Designer Certification Team

"We are very excited to be working with EPTAC Corporation and the marriage of our combined reputations in the market, to support and deliver programs that advance the skills of PCB designers everywhere," noted Gary Ferrari, president of FTS.

8 Cadence Reports Q4, FY 2013 Financial Results

"In 2013, our talented development teams delivered six new innovative products, revenue grew 10%, and we completed three important acquisitions in the IP space," said Lip-Bu Tan, president and CEO. "Our differentiated design IP portfolio led to wins at over ten top tier customers, including head-to-head wins at advanced FinFET nodes."

9 Dr. Cliff Hou to Keynote 51st DAC

Cliff Hou, Ph.D., will be a keynote presenter at the Design Automation Conference, June 1-5, 2014. He will discuss how the introduction of 10nm and 7nm processes will alter today's ecosystem while opening greater EDA and IP opportunities, and will present new system and chip designs.

10 IEEE Reveals "CES: What's Next" Game Results

While many are touting the future as the age of machine control and robots, 75% of the top predictions selected by survey participants skewed toward the desire for mind or movement control in four categories of up-and-coming technologies: Smart appliances, exoskeletons, curved screens on cellphones, and 3D printers.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

MD&M West Conference
February 10–13, 2014
Anaheim, California, USA

Pan Pacific Microelectronics Symposium
February 11–13, 2014
The Big Island, Hawaii, USA

Dallas Expo & Tech Forum
March 4, 2014
Plano, Texas, USA

NORDIC HDI 2014
March 5–6, 2014
Copenhagen, Denmark

Houston Expo & Tech Forum
March 6, 2014
Stafford, Texas, USA

SMTA Webtorial: Tin Whiskers—All You Should Know
March 11, 2014

IPC APEX EXPO—Conference & Exhibition
March 25–27, 2014
Las Vegas, Nevada, USA

Electronics New England
March 26–27, 2014
Boston, Massachusetts, USA

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

PUBLISHER: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER ART: **RON MEOGROSSI**

THE pcb design MAGAZINE

February 2014, Volume 3, Number 2 • The PCB Design Magazine© is published monthly, by BR Publishing, Inc

ADVERTISER INDEX

Coming Soon to *The PCB Design Magazine:*

March:
Documentation:
Why is it Important?

April:
PCB Design
Mythbusting

May:
Design For
Manufacturing